

FEC Considerations for 400GE and Beyond

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Overview

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- Caveats
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- Background
- Next Steps

Motivation

- Reed Solomon used in 100GE, likely to find use in 400GE
- This presentation is to give confidence that we have not reached end point in direct implementation of Reed Solomon
- Show that published algorithms, current commercial devices are enough to deliver Reed Solomon for the foreseeable future
 - Multi-Tbps monolithic performance

Caveats

- This presentation does not suggest that Reed Solomon is the best FEC for future standards
 - Only that it can scale to much higher speeds easily
- Monolithic FEC may not be the best approach
 - Monolithic FECs required for multi-Tbps aggregation
 - Alternate approach may distribute FECs across multiple links

FPGA Technology Scaling

- 40nm FPGA – 2009 production
 - 100K 6LUT (mid range) – 250K 6 LUT (high end)
 - 2.5 Tbps @ 40K 6LUT
 - Normalized 100 Gbps = 1.6K 6LUT
 - Normalized 400 Gbps = 6.4K 6LUT
- 28nm FPGA – 2012 production
 - 200K 6LUT – 400K 6LUT
- 20nm FPGA – 2015 production
 - 200K 6 LUT – 500K 6LUT
- FinFET FPGA – 2017 production
 - 500K 6LUT – 1M 6LUT

N.B. handwaving numbers – to show practicality of implementing future performance in currently available or planned devices

Cauchy Matrix Based Encoding

- **Common Encoding:**

- $p(x) + x^{(n-k)}m(x) = c(x)$
- $p(x)$ is the remainder of the division of $x^{(n-k)}m(x)$ by $g(x)$
- Finding $p(x)$ requires a division circuit (very difficult to parallelize!)

- **Matrix based Encoding**

- RS generator matrix has a Vandermond structure e.g $\mathbf{G} =$
- It can be put in systematic form as: $\tilde{\mathbf{G}} = \mathbf{V}^{-1}\mathbf{G} = [\mathbf{I} \quad \mathbf{P}]$
- Encoding is performed by direct multiplication $\mathbf{c} = \mathbf{m} \cdot \tilde{\mathbf{G}}$

$$\mathbf{G} = \begin{bmatrix} \alpha^{254} & \alpha^{253} & \dots & \mathbf{1} \\ \alpha^{2.254} & \alpha^{2.253} & & \vdots \\ \vdots & \vdots & & \vdots \\ \alpha^{239.254} & \alpha^{239.253} & \dots & \mathbf{1} \end{bmatrix}$$

- **Seroussi encoder¹**

- Systematic generator matrix indices are: $p_{ij} = \frac{\alpha^{i-k-j} \prod (\alpha^{n-1-k-j-t} - \alpha^{n-1-t})}{\alpha^{n-i-1} + \alpha^{n-k-j-1} \prod_{t \neq i} (\alpha^{n-1-i-t} - \alpha^{n-1-t})}$
- With a *relatively* simple recurrence relation between p_{ij} and p_{i+1j} leading to a possible systolic architecture

[1] G.Seroussi, IEEE Trans. on Inf. Theory, Vol.137, no.4,1991

Next Steps

- Other encoder design examples (KP4)
- Multi-Tbps Decoder

Conclusions

- Reed Solomon is scalable to multi-Tbps applications
 - No new FPGA technology required
 - Next generation FPGA technology will be even faster, more cost effective
 - Will work in any technology (such as ASIC)
- Effective – low area/performance ratio
- Low latency

Thank You