FEC Codes for 400 Gbps 802.3bs

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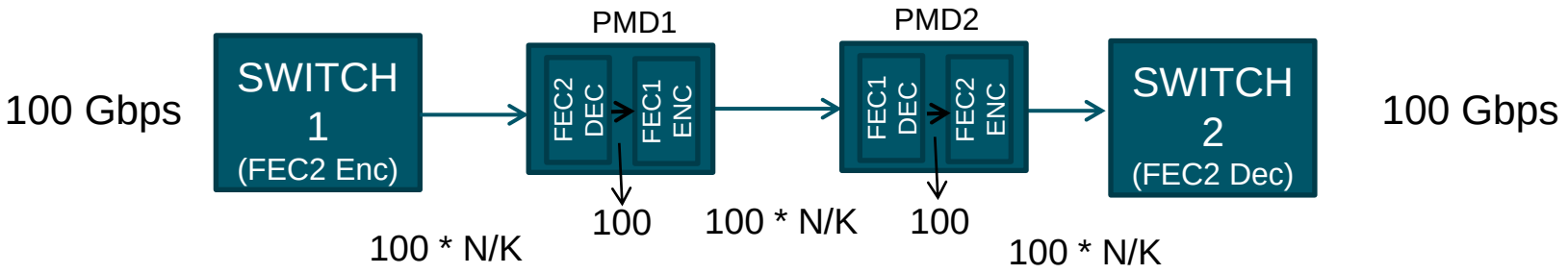
FEC CODES FOR 400G

- **A number of FEC options are being discussed for 400Gbps standard**
- **These include RS codes from the 802.3 bj (KR4 and KP4), BCH codes and MLC codes**
- **Presentation will explore performance tradeoffs for these codes with emphasis on BCH and RS codes**
  - Help guide choice of code

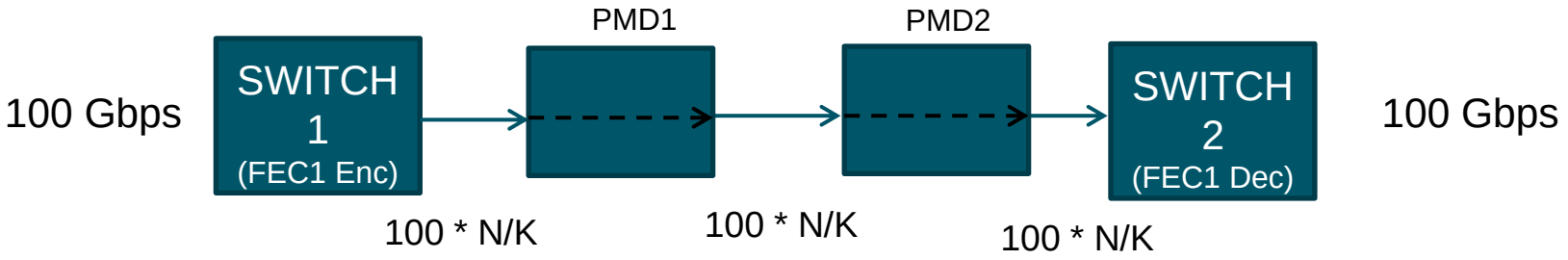
FEC APPLICATION: MULTI-FEC SUPPORT WITH SINGLE LINE RATE AND OPTIONAL PASS-THROUGH

FEC1: (N, K) code
FEC2: Another code choice with the same N/K overhead (with lower gain/latency)

Regular Mode



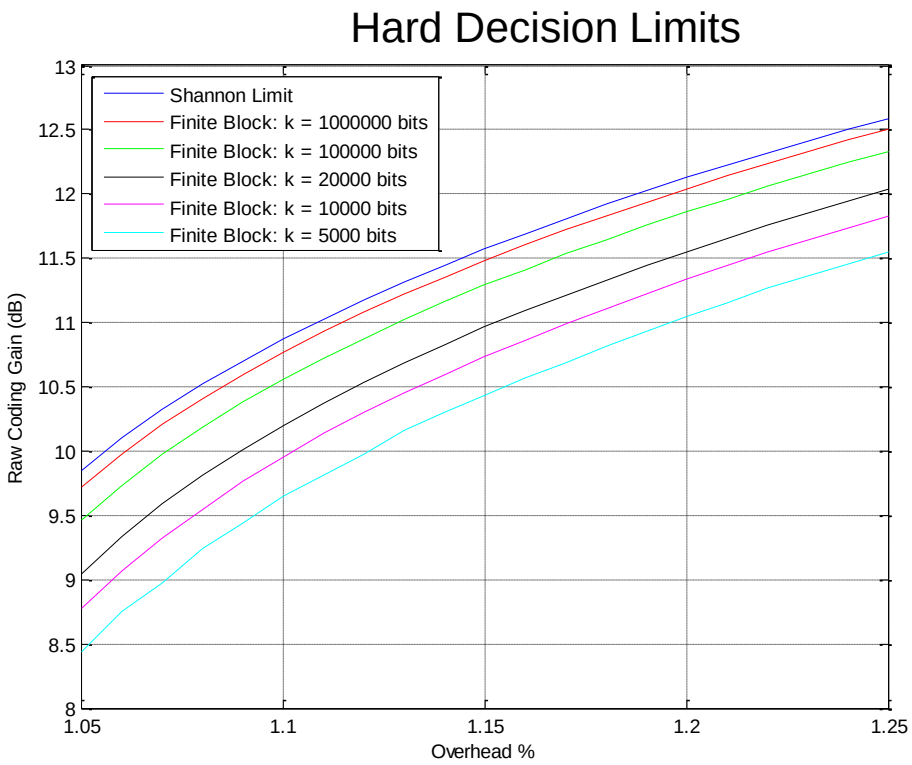
Pass-through Mode



User choice on which FEC to implement
With single line rate, PLL supports only a single line rate
Alternate Solution: Use different rate code (e.g., KR4, KP4 RS code) for FEC2 which would require a line rate change

Example Code: BCH(2864,2570)
RS(179,161, m=8)

FEC CODING GAIN AT 1E-15 VS. OVERHEAD

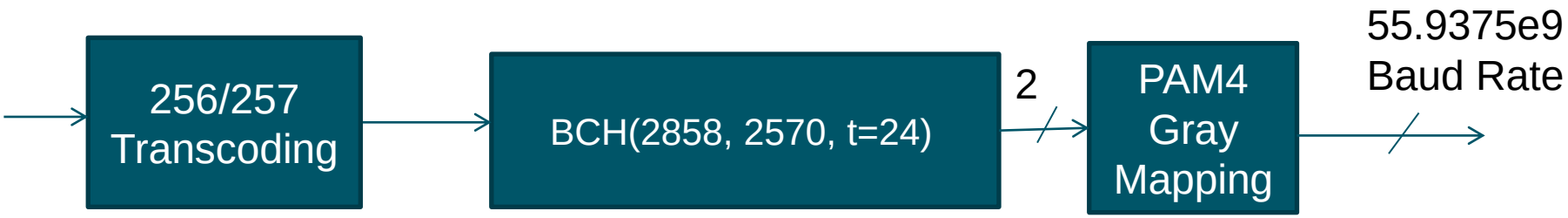


- Hard decision FEC limit is 11dB coding gain for 56GBaud PAM4
  - 12% overhead
  - <100ns latency requirements reduces the coding gain limit to 9dB
- MLC codes can provide further coding gain or lower complexity (at similar gain) if required

  Example 1: LSB: BCH(N=1432, K =1179, t=23), MSB: BCH(N=1432, K = 1399, t=3)
  Example 2: LSB: RS (N=288, K=240, t=24), MSB: RS (N=528, K=514, t=7).

BCH CODE WITH HIGH GAIN / LOW LATENCY

Choice of FEC code parameters involves a triple tradeoff
– Latency
– Coding gain
– Over clocking (higher Baud rate)

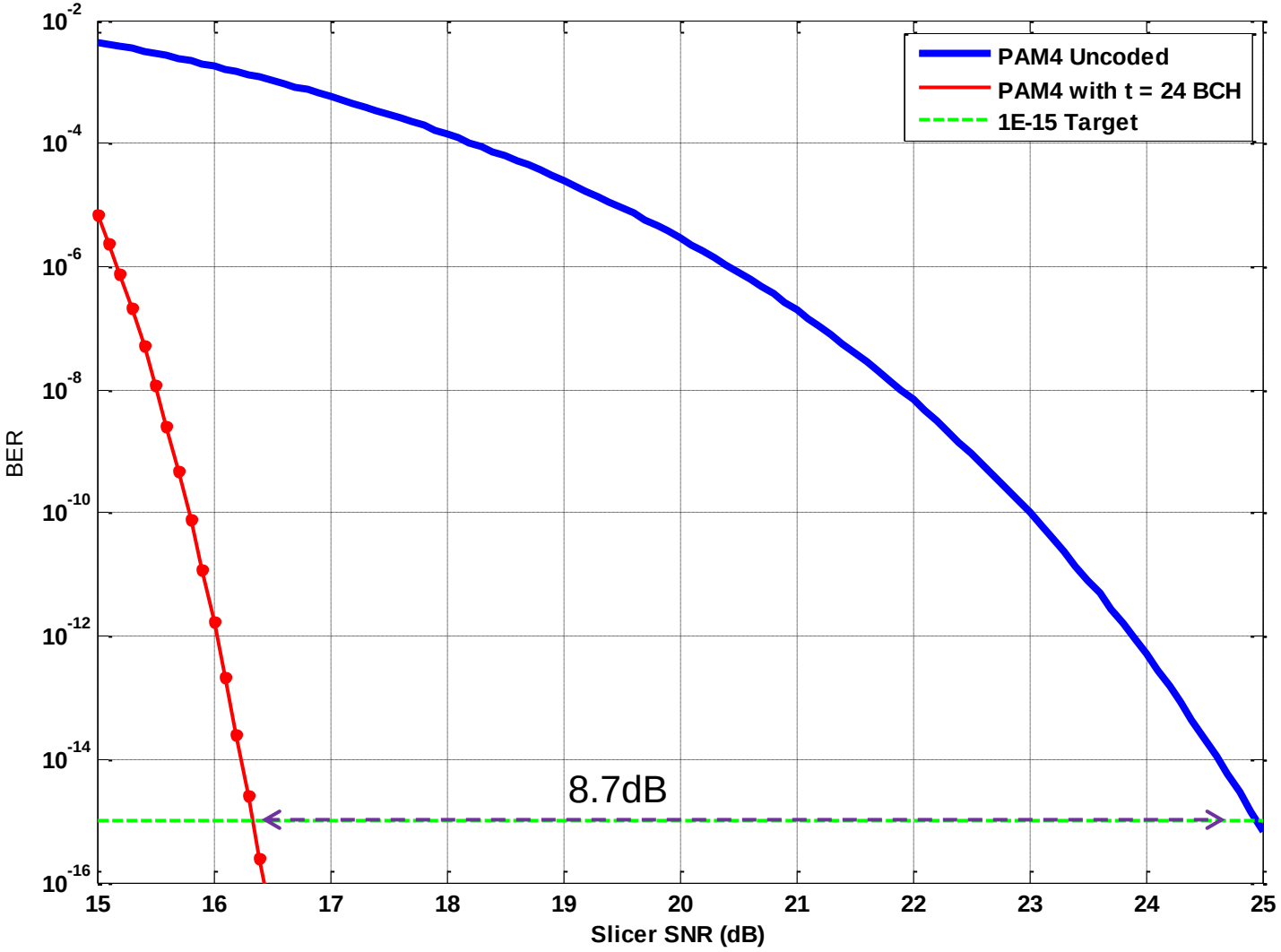


- Gray Mapping, 6 additional parity bits are available.
- Ethernet Rate = 2864 / 2570 * 257/256 * 100 / 2 = 55.9375e9
- Input Error Rate = 1.25E-3, Output Error Rate = 1E-15
- PAM4 SNR = 16.3dB, Coding Gain = 8.7dB
- Lower gain FEC code at same rate: RS(179, 161, t=9, m=8), Coding Gain = 6.9 dB

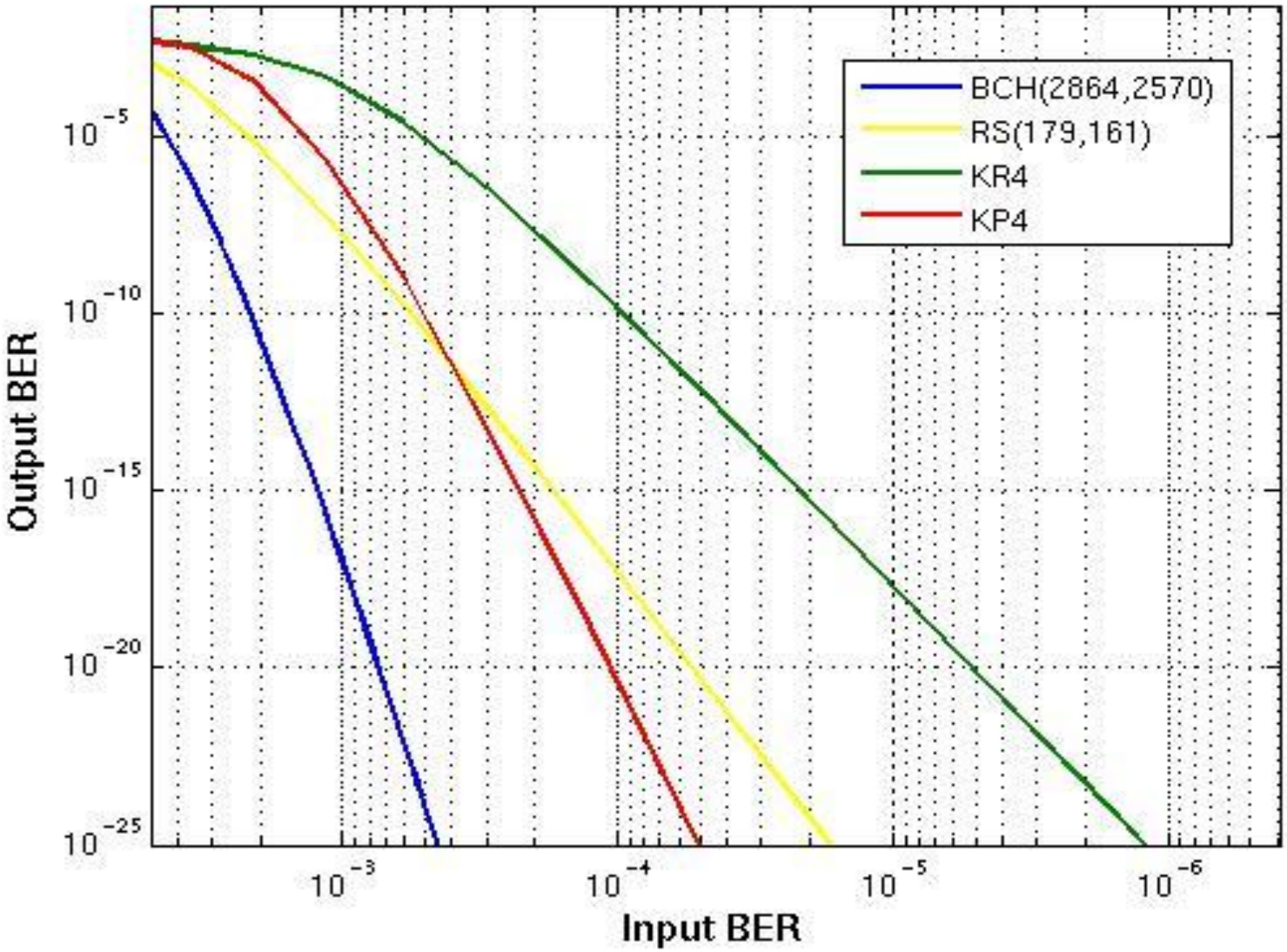
PROPOSED BCH FEC DETAILS

- **100G Intrinsic FEC Block latency is 26ns.**
  - 802.3bj KR FEC is 51ns
  - ½ the latency of 802.3bj RS(528,514) KR FEC
- **400G block latency is ~7ns**
- **Total processing latency is 50ns**
  - Processing latency is similar for 100G or 400G.
- **Total FEC latency is 75ns, 100ns with error marking**
- **Rate is 358 x reference clock of 156.25MHz**

BCH FEC PERFORMANCE

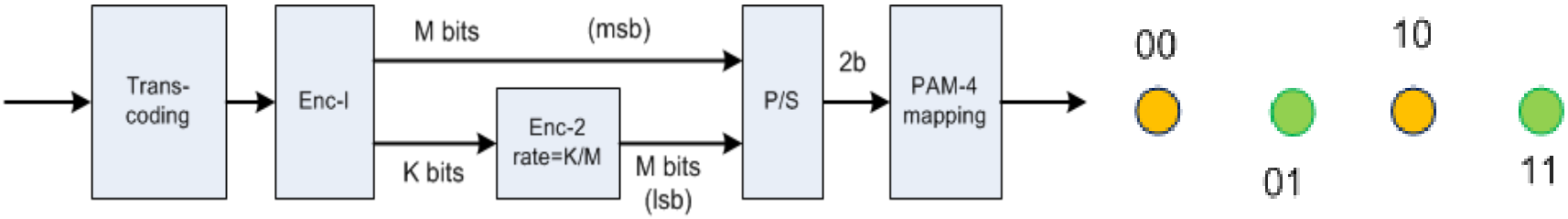


FEC CODE PERFORMANCE

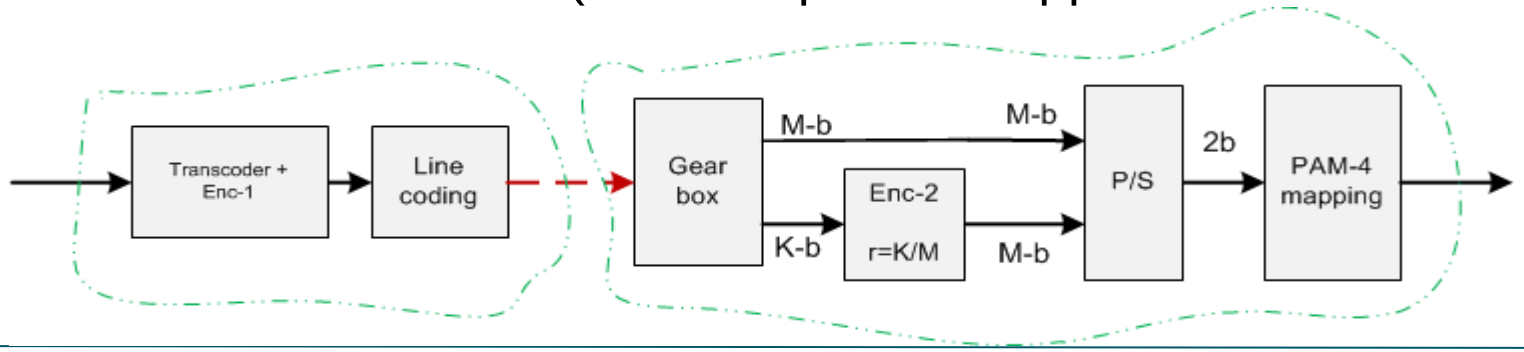


MLC CODE EXAMPLE

- RS MLC Code example:
  - Code-1: RS(528, 514, t=7)
  - Code-2 daughter code: RS(144, 120, t=12) (optional)
  - Code-2 mother code: RS(288, 240, t=24)
  - Overall OC=9.09%, M=72, K=60 (refer to figure below)
  - Coding gain: ~ 8.5 dB
  - Power: < 3.5X KR4-FEC



- Distributed MLC structure (Another possible application methodology*)



*A special case of segmented FEC application (further information in backup)

http://www.ieee802.org/3/bs/public/adhoc/logic/oct21_14/wangz_01_1014_logic.pdf

FEC CODE TRADE-OFFS (ASSUMING SIMILAR CODE RATE)

Code	Delay	Power** (baselined to KR4)	Random Coding Gain	Burst Error Correction
BCH	< 100 ns	~8x##	High	Moderate
RS*	< 50 ns	~1.5x	Moderate	High
MLC	< 120 ns	~3.5x	High	Moderate-High#

* Note: KP4 has similar performance at a higher latency

**Note: Assume innovative decoders to reduce power

#Note: Depends on component codes

##Note: The power estimation may be pessimistic. Further power savings (~4-5x) could potentially be achieved by more advanced decoder design

FEC CODE TRADE-OFFS (CONT'D)

Code	Input BER	Overclocking ratio)	Random Coding Gain
BCH	1.2e-3	~ 8.5%	~8.7dB*
RS	1.7e-4	~ 8.5%	~6.9dB*
MLC (BCH)	2.2e-3	~ 8.5%	~8.6dB**
MLC (RS)	1.3e-3	~ 9.1%	~8.5dB**

*Gray coding and PAM4 modulation were assumed

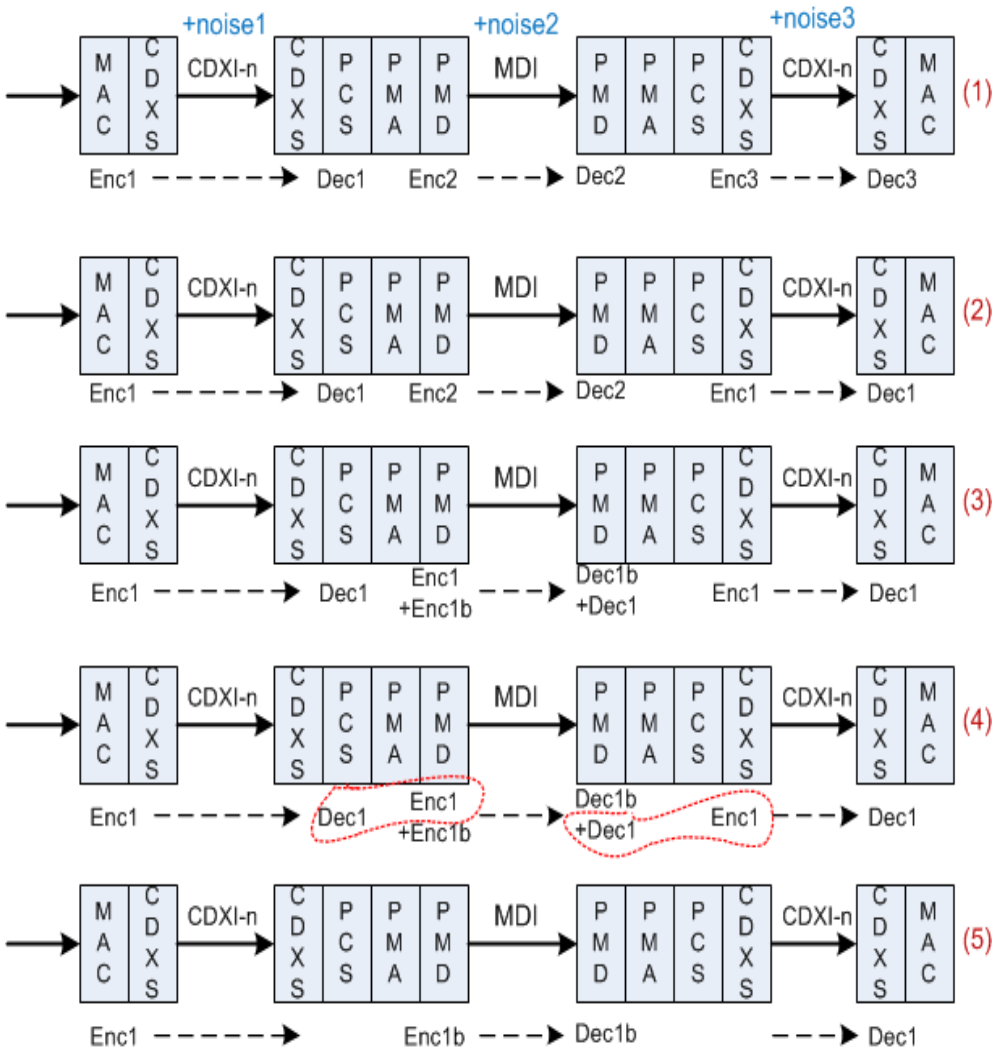
**PAM4 modulation was assumed

CONCLUSION

- **A number of options have been presented for the 802.3bs standard**
  - Analyzed tradeoffs for multiple families of block codes
- **High coding gain FEC's are available at reasonable delay/complexity for 400Gbps applications**
  - Complexity/delay tradeoffs presented here can guide picking specific code
- **MLC is an attractive option for applications requiring high coding gain**

Backup (Additional Information)

FURTHER SIMPLICATIONS IN FEC APPLICATION



1) Typical *segment-to-segment* FEC structure

(2) Simplification: make code1=code3 making it symmetrical

(3) A special case of (2): use MLC for code2. Select outer code=code1, the 2nd portion of MLC is denoted as Enc1b in the figure

(4) Merge "Decoder-1 and encoder-1" operation at module side. This is equivalent to correcting all errors without removing parity data

(5) One more step simplification based on (4): cancel "Dec1+Enc1" operation in module. This creates a distributed MLC scheme*

*http://www.ieee802.org/3/bs/public/adhoc/logic/oct21_14/wangz_01_1014_logic.pdf