

56G NRZ Measured Test Results

(in support of Chip to Module and Chip to Chip Interfaces)

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50G NRZ Measurements

➤ Objectives:

- Generate test result data to support 56G NRZ channel loss greater than the chip to module interface specification
- Generate test result data to support extending 56G NRZ to the chip to chip interface specification

➤ Results: Demonstrated 50G NRZ greater than 30dB

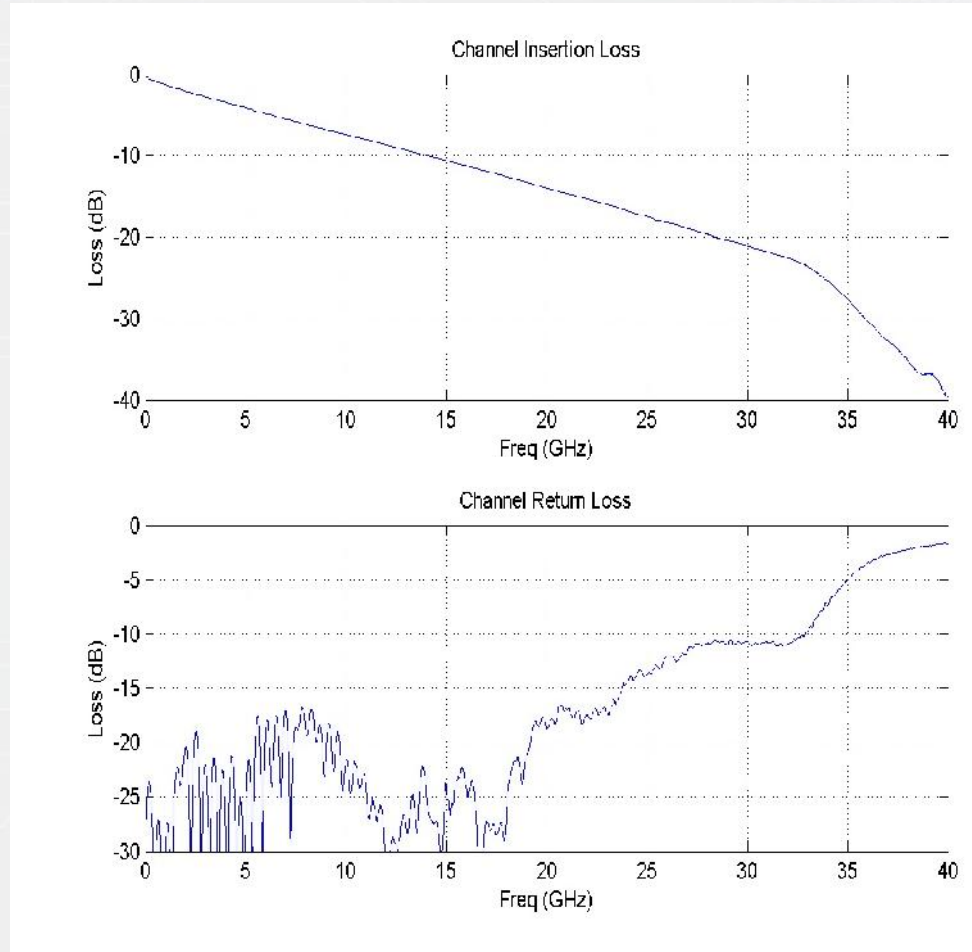
- Note #1: Equalization numbers do not include the Tx and Rx channel loss from the Credo evaluation board or the breakout cables to the test channels.
- Note #2: Measured result are without FEC

Speed	Pattern	Error Rate	Trace Length	Eye Margin
50G	PRBS31	<1e-13	7.3in (-17.55dB)	197.66mV

The screenshot shows the VoltMonitor software interface with the following configuration details:

- Data:** Volt Monitor button; Agc: 1, 4, 3; Link: 1; Prbs: 0000 (circled); Err Gen; Err Clear; Freq Off: 0 ppm; Eye Margin: 197.66 mv.
- Adaption:** Adaptation Start; Adaptation Freeze.
- PRBS:** Internal Loopback; TX_1T_Pattern; TX_2T_Pattern; TX_4T_Pattern; TX_8T_Pattern; TX_PRBS7; TX_PRBS15; TX_PRBS21; TX_PRBS31 (selected).
- Emphasis:** Pre-Emphasis: 10; Post-Emphasis: 6; TX Swing: 100 %.
- Control:** WRITE 8 READ 11FF WRITE; WRITE 3b READ 0000 WRITE; WRITE 0 READ 0 WRITE.

An eye diagram window titled 'Figure 1' is visible in the bottom left, showing a clear signal waveform with a voltage range from -200 to 200 and a time range from -0.4 to 0.4.

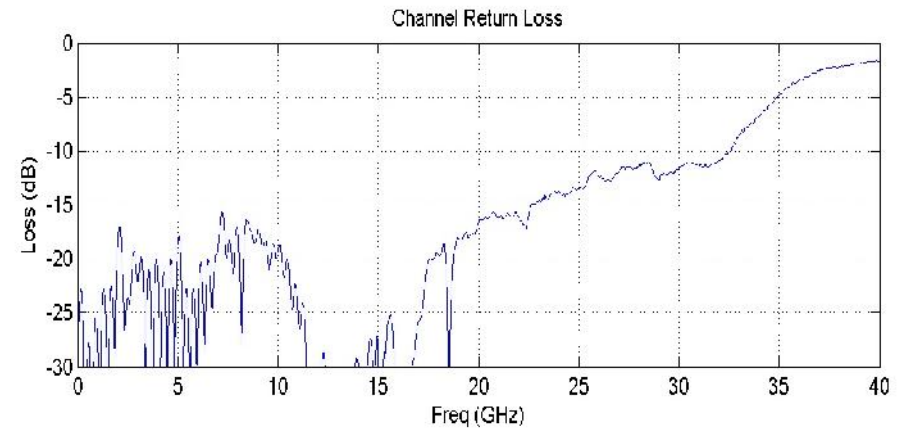
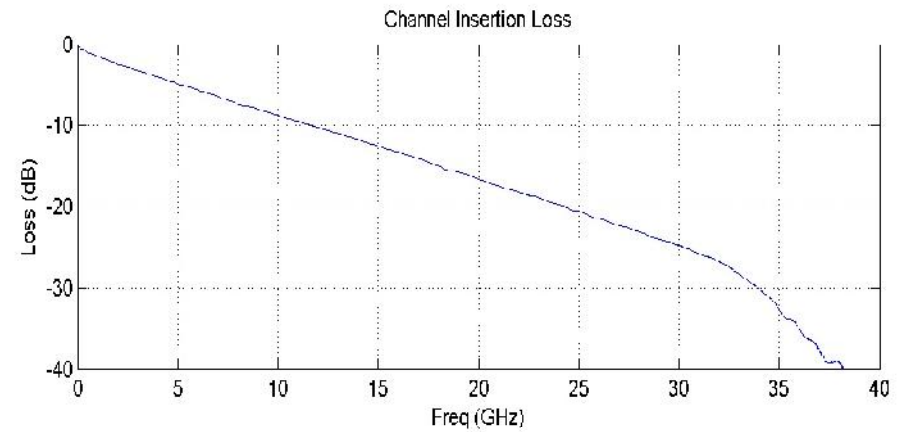


Speed	Pattern	Error Rate	Trace Length	Eye Margin
50G	PRBS31	<1e-13	8.7in (-20.78dB)	140.41mV

The screenshot shows the VoltMonitor software interface. The main configuration area includes:

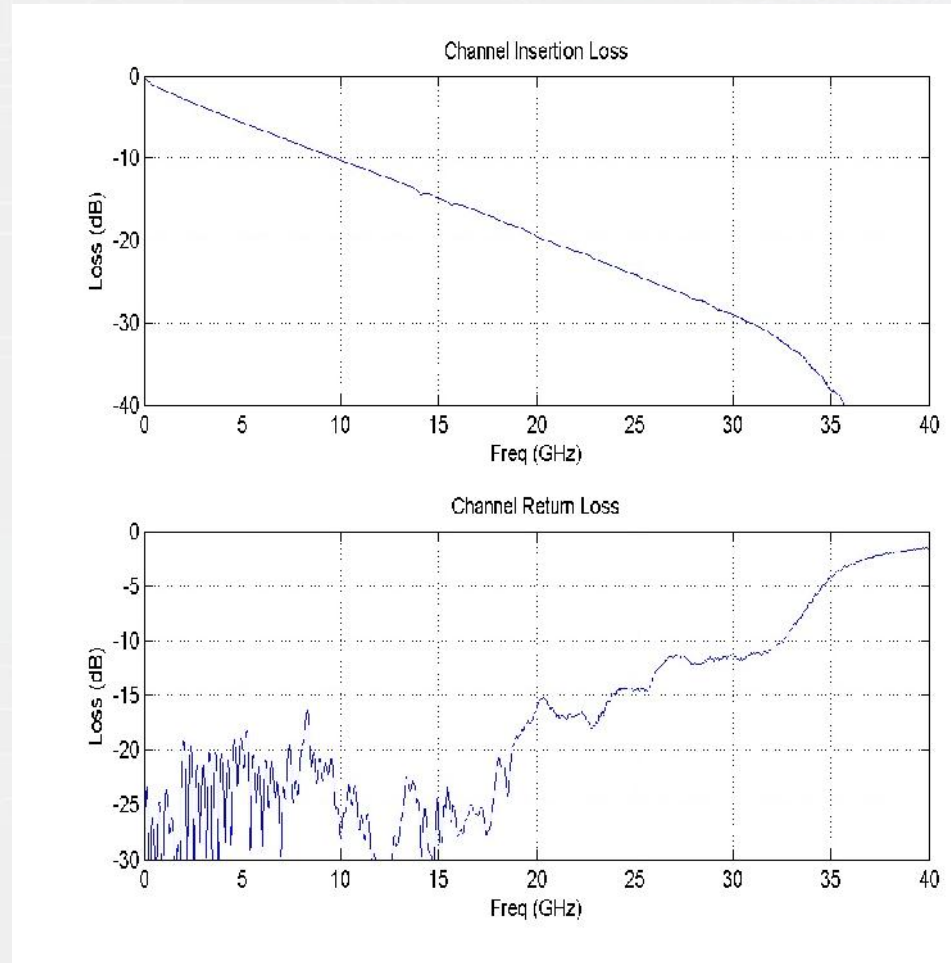
- Data:** Volt Monitor button, Agc (1, 5, 3), Link (1), Prbs (0000, circled), Err Gen, Err Clear, Freq Off (0 ppm), Eye Margin (140.41 mv).
- Adaption:** Adaptation Start, Adaptation Freeze.
- PRBS:** Internal Loopback, TX_1T_Pattern, TX_2T_Pattern, TX_4T_Pattern, TX_8T_Pattern, TX_PRBS7, TX_PRBS15, TX_PRBS21, TX_PRBS31 (selected).
- Emphasis:** Pre-Emphasis (10), Post-Emphasis (6), TX Swing (100 %).
- Registers:** WRITE 8 READ 11FF WRITE, WRITE 3b READ 0080 WRITE, WRITE 0 READ 0 WRITE.

In the bottom left, a window titled 'Figure 1' displays an eye diagram showing Voltage (mV) on the y-axis (ranging from -200 to 200) and Time (U) on the x-axis (ranging from -0.4 to 0.4). The eye diagram shows a clear signal with a central blue region and red/orange background.



Speed	Pattern	Error Rate	Trace Length	Eye Margin
50G	PRBS31	<1e-13	10.2in (-24.43dB)	91.41mV

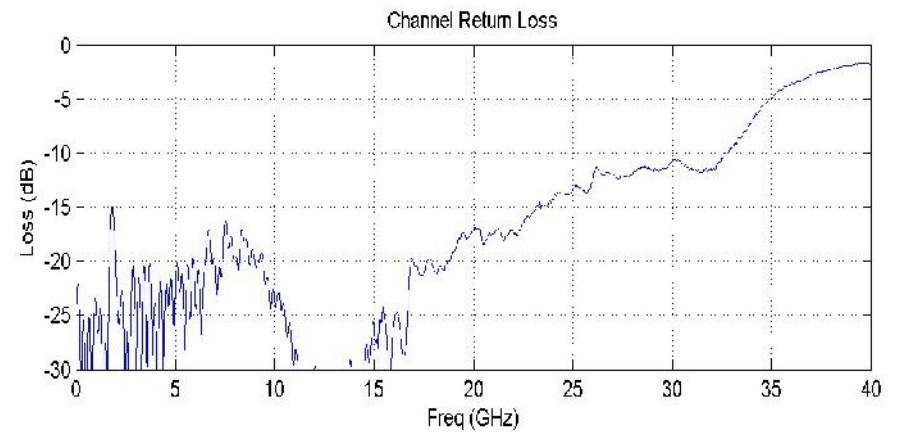
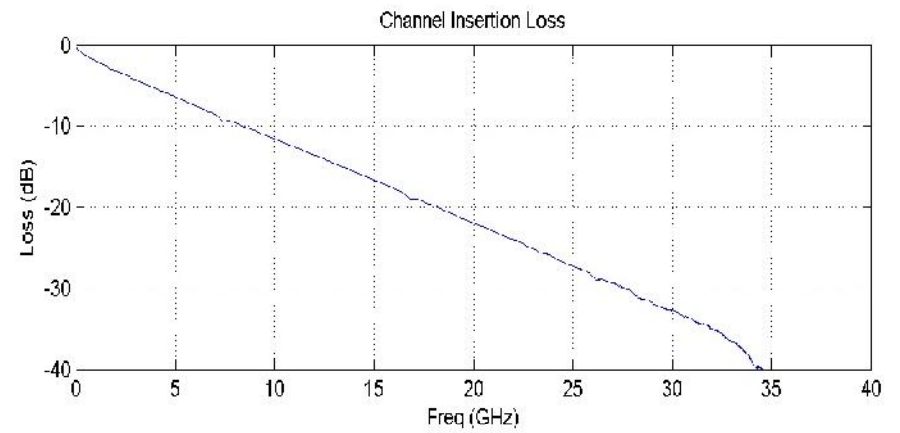
The screenshot shows the VoltMonitor software interface. The 'Data' section includes a 'Volt Monitor' button, 'Agc' settings (1, 4, 3), 'Link' (1), 'Prbs' (0000, circled), 'Err Gen', 'Err Clear', 'Freq Off' (0 ppm), and 'Eye Margin' (91.406 mv). The 'Adaption' section has 'Adaptation Start' and 'Adaptation Freeze' buttons. The 'PRBS' section lists various patterns, with 'TX_PRBS31' selected. The 'Emphasis' section shows 'Pre-Emphasis' (10), 'Post-Emphasis' (14), and 'TX Swing' (100%). At the bottom, there are 'WRITE' and 'READ' buttons for hex values 8, 3b, e5, 11FF, 0080, and 0003. An eye diagram is visible in the bottom-left corner, showing a signal waveform with a central eye opening.



Speed	Pattern	Error Rate	Trace Length	Eye Margin
50G	PRBS31	~6e-13	11.68in (-27.49dB)	77.93mV

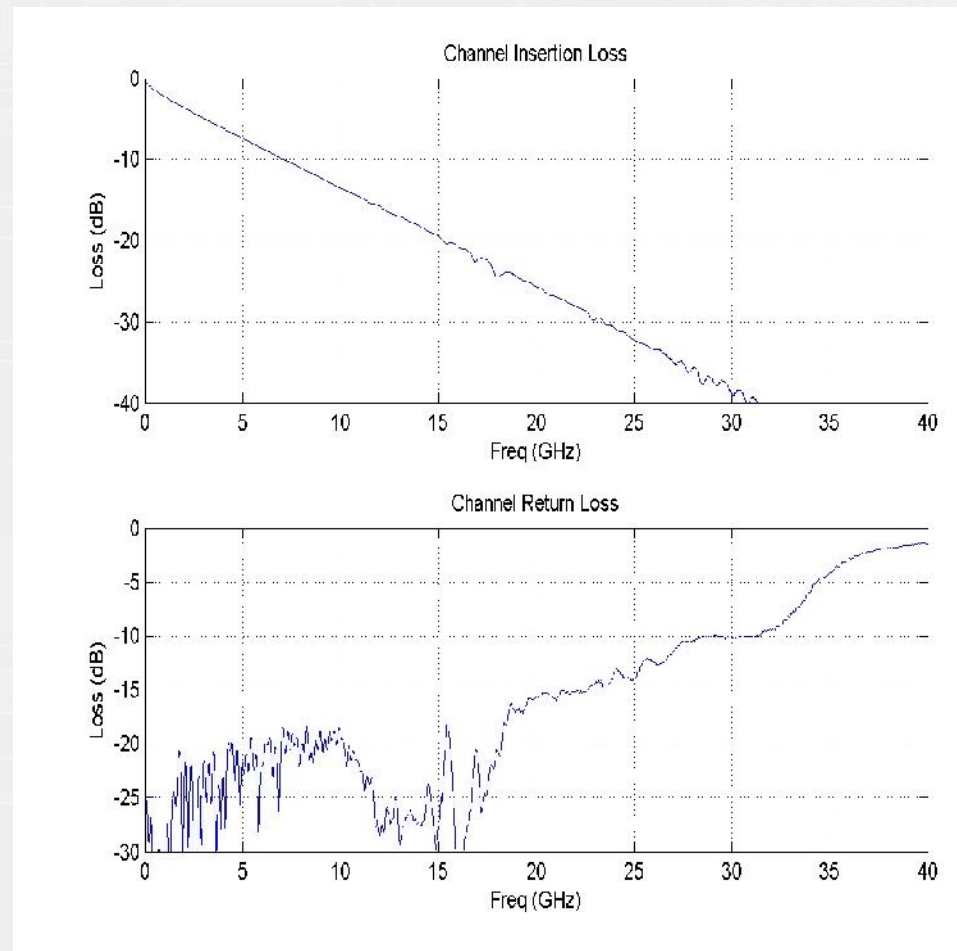
The screenshot shows the VoltMonitor software interface. The 'Data' section includes a 'Volt Monitor' button, 'Agc' settings (1, 4, 1), 'Link' (1), 'Prbs' (000a, circled), 'Err Gen', 'Err Clear', 'Freq Off' (0 ppm), and 'Eye Margin' (77.93 mv). The 'Adaption' section has 'Adaptation Start' and 'Adaptation Freeze' buttons. The 'PRBS' section shows 'Internal Loopback' and various pattern options, with 'TX_PRBS31' selected. The 'Emphasis' section includes 'Pre-Emphasis' (16), 'Post-Emphasis' (10), and 'TX Swing' (100 %). At the bottom, there are 'WRITE', 'READ', and 'WRITE' buttons for different data patterns.

Figure 1 shows an eye diagram with 'Voltage (mV)' on the y-axis (ranging from -150 to 150) and 'Time (ns)' on the x-axis (ranging from -0.4 to 0.4). The diagram displays a clear signal with a central eye opening.



Speed	Pattern	Error Rate	Trace Length	Eye Margin
50G	PRBS31	~1e-10	13.1in (-31.41dB)	65.63mV

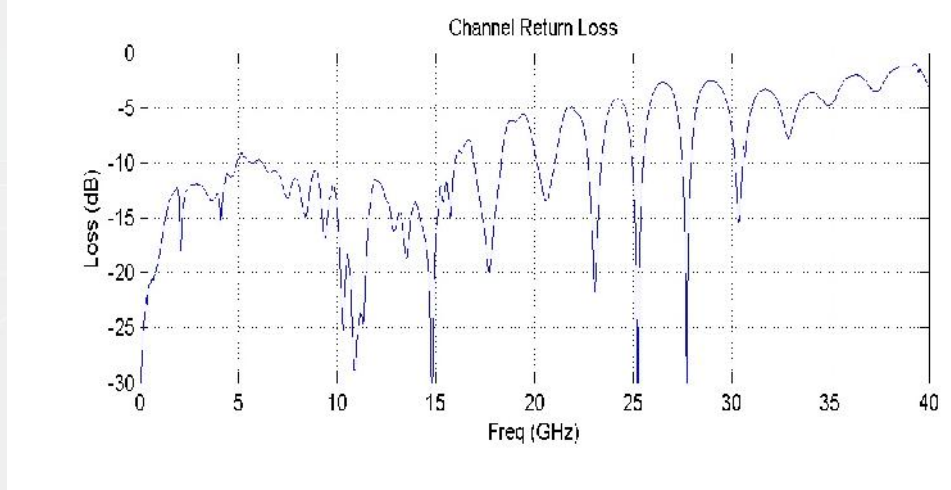
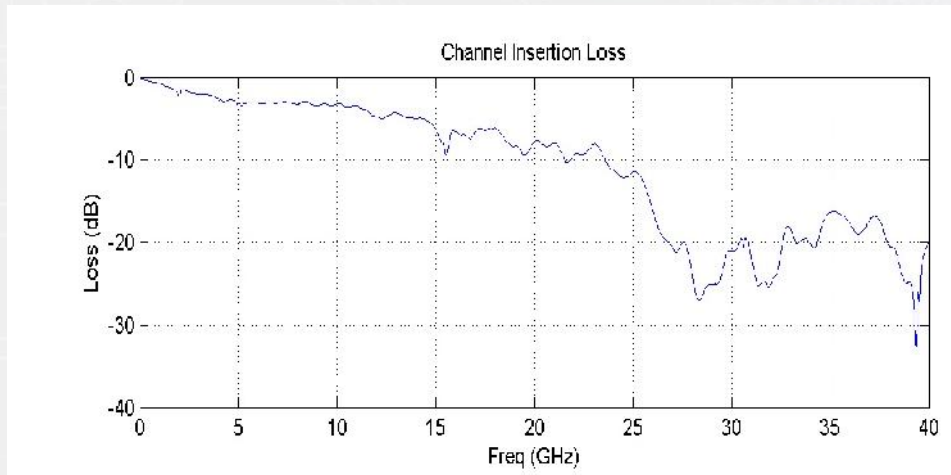
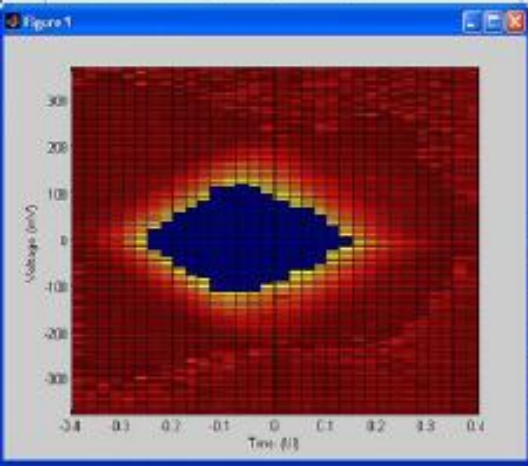
The screenshot shows the VoltMonitor software interface. The 'Data' section includes a 'Volt Monitor' button, 'Agc' (1, 3, 1), 'Link' (1), 'Prbs' (0110, circled), 'Err Gen', 'Err Clear', 'Freq Off' (0 ppm), and 'Eye Margin' (65.625 mv). The 'Adaption' section has 'Adaptation Start' and 'Adaptation Freeze' buttons. The 'PRBS' section lists various patterns, with 'TX_PRBS31' selected. The 'Emphasis' section shows 'Pre-Emphasis' (16), 'Post-Emphasis' (4), and 'TX Swing' (100%). At the bottom, there are 'WRITE', 'READ', and 'WRITE' buttons for addresses 61, 9, 05, 7020, 0000, and 0003. An eye diagram is visible in the bottom-left corner, showing a clear signal with a central blue region and red background.



Speed	Pattern	Error Rate	Trace Length	Eye Margin
50G	PRBS31	<1e-13	HCB-MCB (-10.38dB)	187.5mV

The screenshot shows the VoltMentor software interface with the following settings:

- Data:** Volt Monitor button.
- Agc:** 2, 4, 3 (dropdowns).
- Link:** 1 (text field).
- Prbs:** 0000 (text field, circled in red).
- Err Gen** and **Err Clear** (buttons).
- Freq Off:** 0 ppm (text field).
- Eye Margin:** 187.5 mv (text field).
- Adaption:** Adaption Start and Adaption Freeze (buttons).
- PRBS:** Internal Loopback (radio button), TX_1T_Pattern, TX_2T_Pattern, TX_4T_Pattern, TX_8T_Pattern, TX_PRBS7, TX_PRBS15, TX_PRBS21, TX_PRBS31 (radio buttons).
- Emphasis:** Pre-Emphasis: 10, Post-Emphasis: 0, TX Swing: 100% (dropdowns).
- WRITE/READ/ERROR:** A grid of buttons for writing and reading error codes (e.g., WRITE 61, READ 0020, WRITE).



Speed	Pattern	Error Rate	Trace Length	Eye Margin
50G	PRBS31	~1e-8	QSFP breakout cards + 3-meter cable (<-30dB)	<50mV

VoltMonitor

Data

Volt Monitor

Agc: 1 4 1

Link: 1

Prbs: b771

Freq Off: 0 ppm

Eye Margin: 118.75 mv

Adaption

Adaptation Start Adaptation Freeze

PRBS

Internal Loopback

TX_1T_Pattern TX_2T_Pattern

TX_4T_Pattern TX_8T_Pattern

TX_PRBS7 TX_PRBS15

TX_PRBS21 TX_PRBS31

Emphasis

Pre-Emphasis: 26

Post-Emphasis: 0

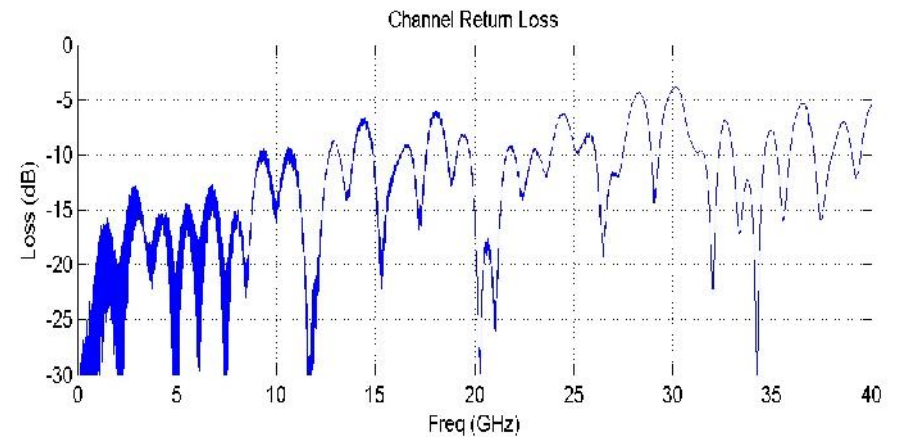
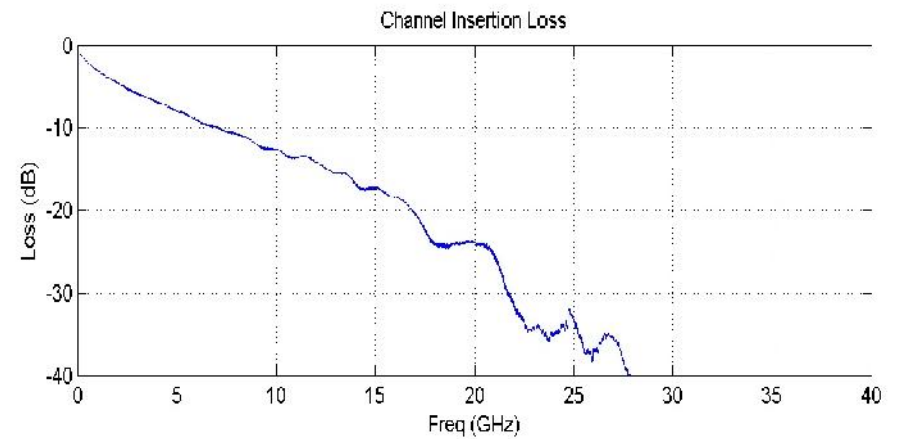
TX Swing: 100 %

WRITE 61 READ 7020 WRITE

WRITE 2 READ 0401 WRITE

WRITE 66 READ D09E WRITE

Figure 1



Summary

- **56Gb/s NRZ is feasible and advantageous for 400GE**
 - CEI-56G VSR, XSR, USR can all be met with margin (30dB+ proven in silicon at 50Gb/s in 40nm)
 - CEI-56G-MR feasible with FEC
 - Power efficient for next generation switch chip designs
 - Provides placement flexibility for OE and backplane drivers
- **Next Steps:**
 - Test more channels in support of baseline proposals for 56G NRZ chip to module and chip to chip specifications