Further information on PAM4 error performance and power budget considerations

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- Brief summary of 2 SMF Ad Hoc presentations on BER-floors
- Information on testing conditions
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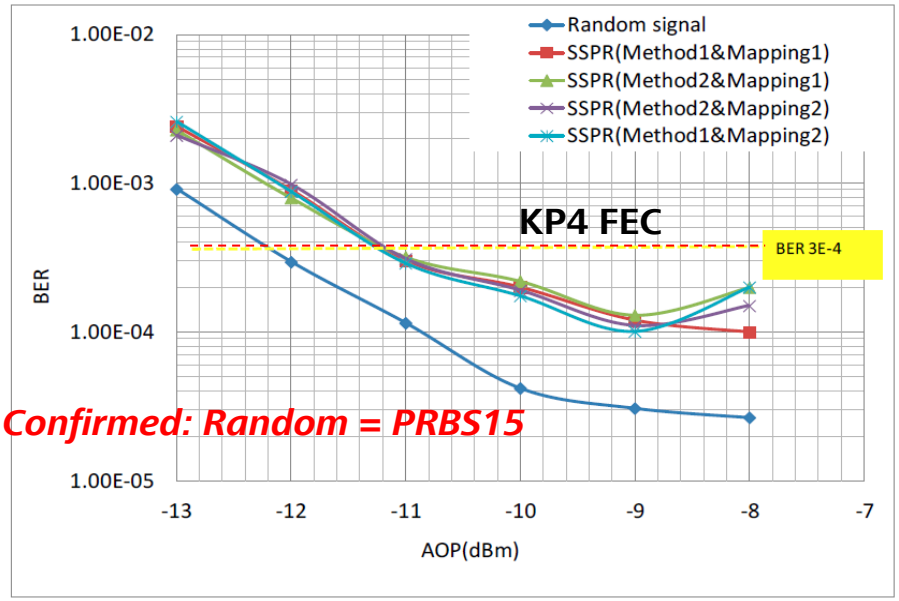
- Q&A

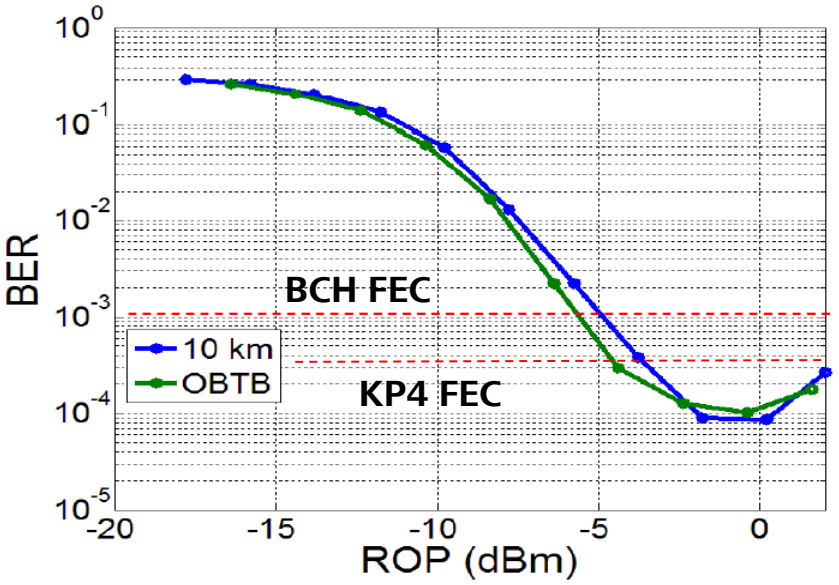
Recap of “stassar_01_1014_smf”, SMF Ad Hoc, 14 Oct 2014

“BER-floors in 400Gb/s Ethernet SMF PMDs, What are the issues?”

- During both San Diego (July 2014) and Ottawa (September 2014) many presentations with test results showing BER curves have been given.
- Some examples for 8x50G PAM4 and 4x100G PAM4



xu_3bs_01_0714



way_3bs_01a_0914

Message from stassar_01_1014_smf

We need to confirm that a BER floor, shown in laboratory test results, close to the FEC operation point, will stay where it is and not move strongly up/down for small variations of operating conditions, to avoid big variations in receiver sensitivity as soon as we add dispersion, jitter, voltage and temperature variations and multi-vendor interworking conditions.

Questions on stassar_01_1014_smf

- Which algorithm was used for performing CDR function in xu_3bs_01_0714?
- What happens if we lower the baudrate in the experiment?
- Where in the SSPR pattern are the errors?
- Where is the “problem”? In the transmitter or the receiver? Is it the BW of the transmitter or jitter on the recovered clock?

CDR algorithm used in xu_3bs_01_0714

Timing recovery: Gardner algorithm

- widespread use
- uses two samples per symbol
- insensitive to carrier offsets, the timing recovery loop can lock first, therefore simplifying the task of carrier recovery.
- error for the Gardner algorithm is computed using the following equation: $e_n = (y_n - y_{n-2})\, y_{n-1}$,where the spacing between y_n and y_{n-2} is T seconds, and the spacing between y_n and y_{n-1} is $T/2$ seconds.
- figures illustrate how the sign of the Gardner error can be used to determine whether the sampling is correct, late or early
- Gardner error is most useful on symbol transitions

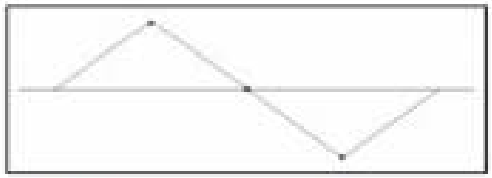


Figure 5.1. Correct timing: $e_n = (-1\ -1) \bullet 0 = 0$.

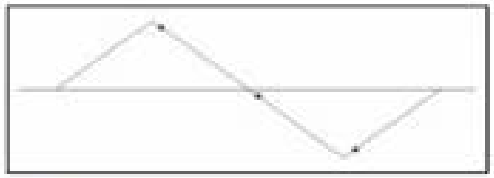


Figure 5.2. Timing is late: $e_n = (-0.8\ -0.8) \bullet (-0.2) = 0.32$.

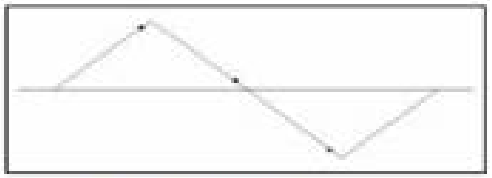
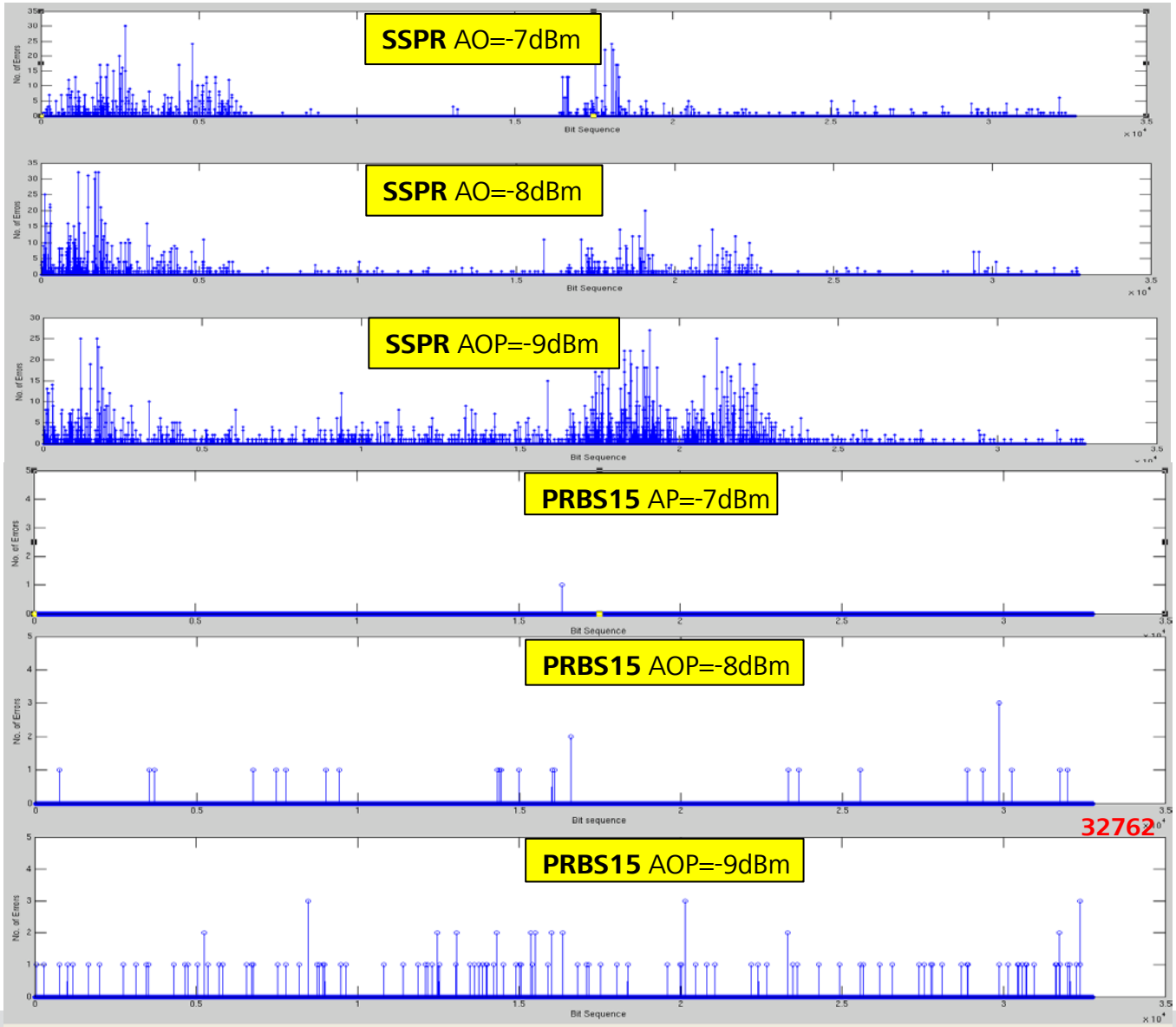


Figure 5.3. Timing is early: $e_n = (-0.8\ -0.8) \bullet (0.2) = -0.32$.

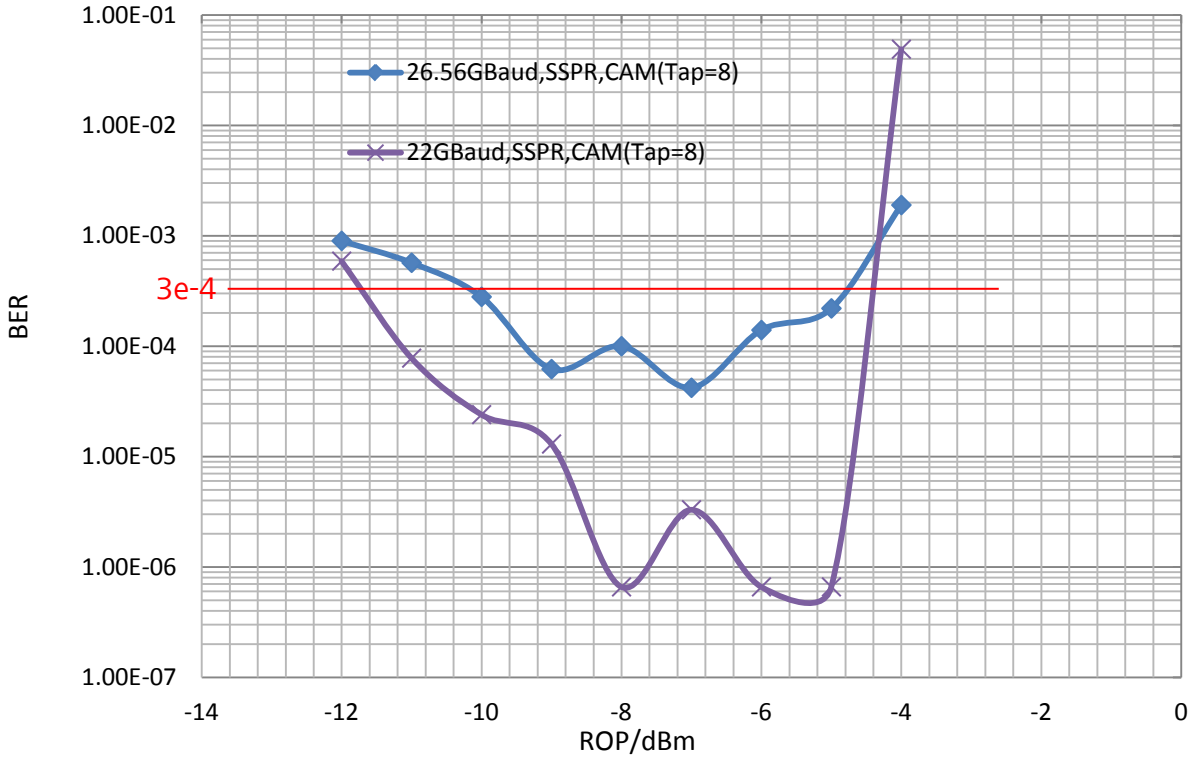
Reference: Postgraduate Course in Radio Communications, Fall 2004 – Spring 2005

Location of errors in the SSPR pattern in xu_3bs_01_0714



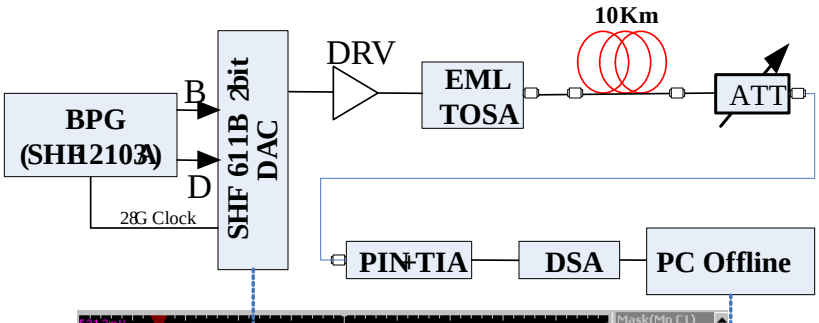
X-axis: bit sequence
Max block size 32762x10^4

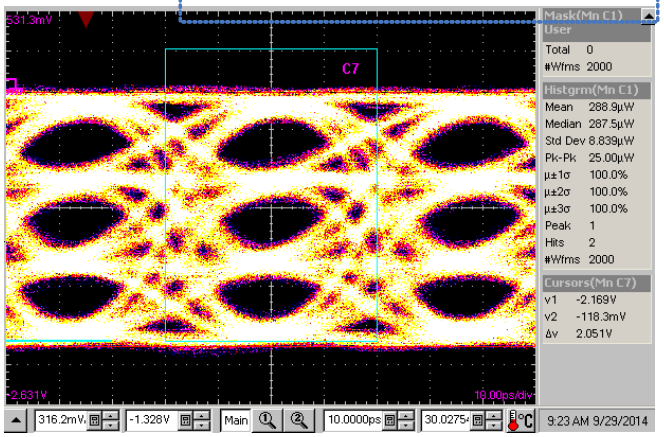
Effects of lowering the baudrate with SSPR testing in 8x50G PAM4 configuration



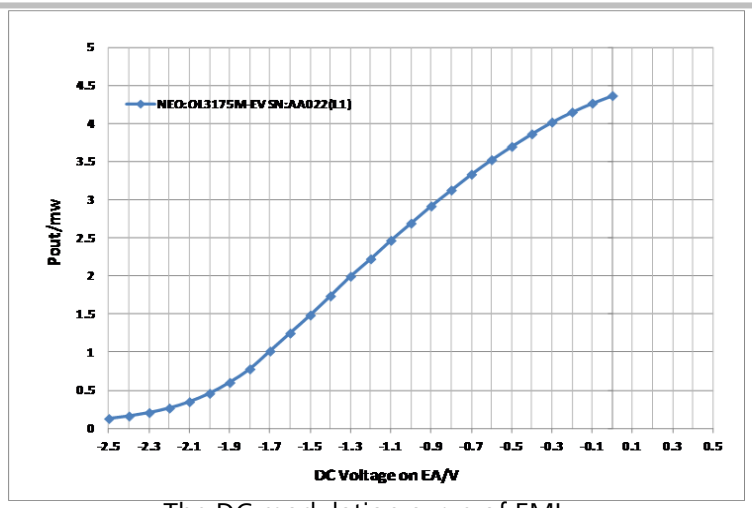
In this further experiment the baud rate was reduced from 26.56Gbd to 22Gbd (SSPR pattern). The BER floor significantly improved demonstrating the relevance of testing with an SSPR pattern

Further testing 56Gb/s PAM4
EML with high bandwidth and linear device



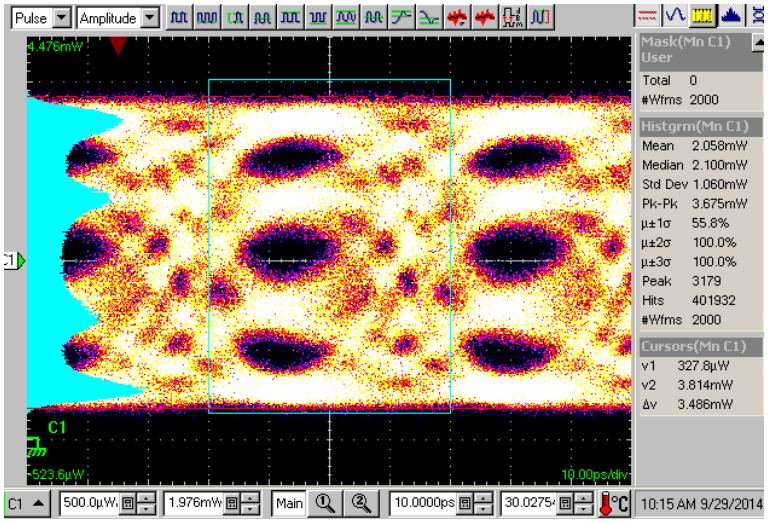


Eye diagram of the signal after SHF 807driver



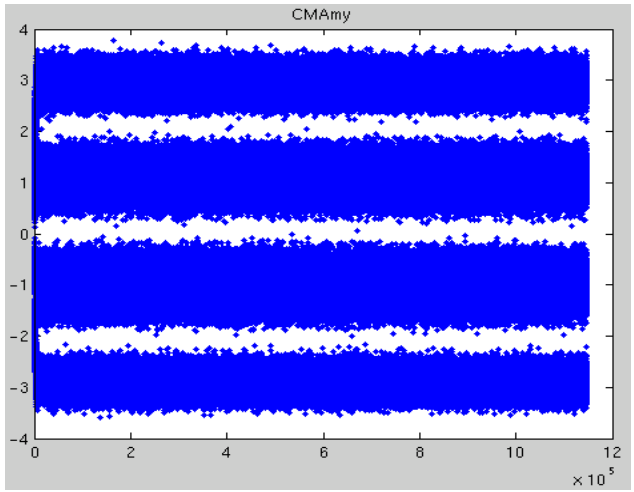
The DC modulation curve of EML

- The devices used in the experiment were selected on highest bandwidth and best linearity.
- ESNR after the driver is about 27dB.
- EML is adjusted to work in its linear region to achieve the widest eye opening
- The modulated optical signal is adjusted to get uniform eye opening. ER is larger than 10dB

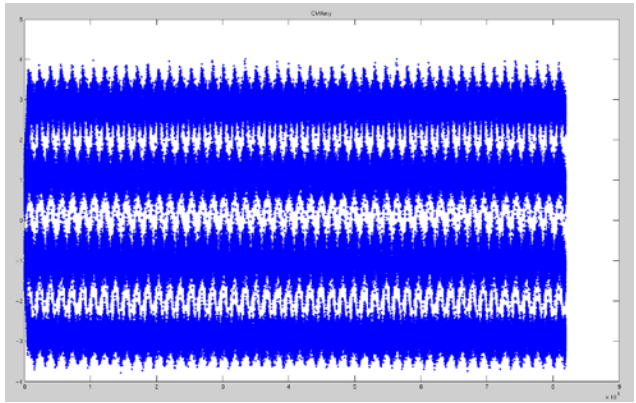


optical eye diagram of the EML

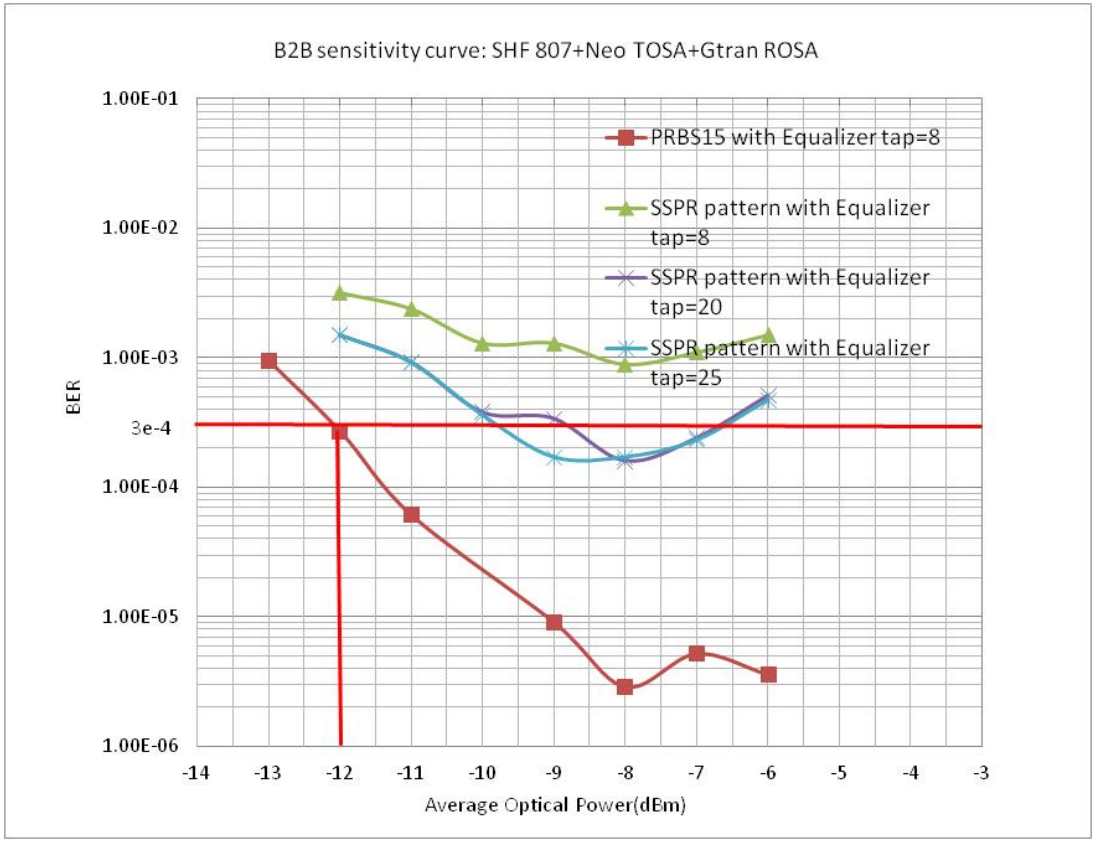
Further testing 56Gb/s PAM4, continued
EML with high bandwidth and linear device



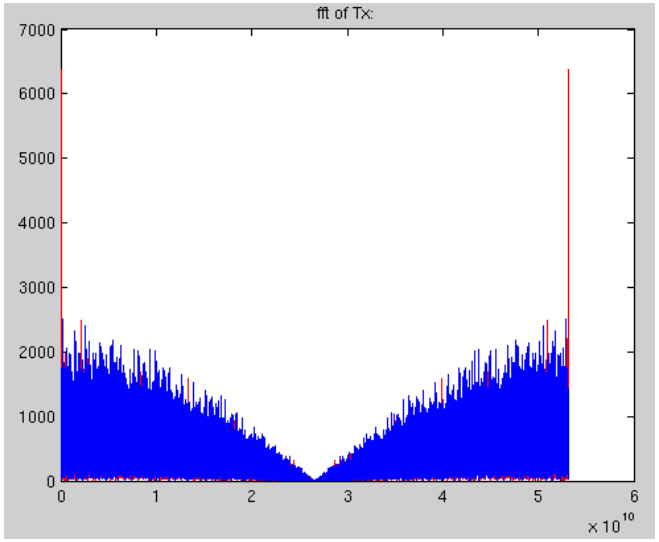
Electrical level distribution after EQ for PRBS pattern



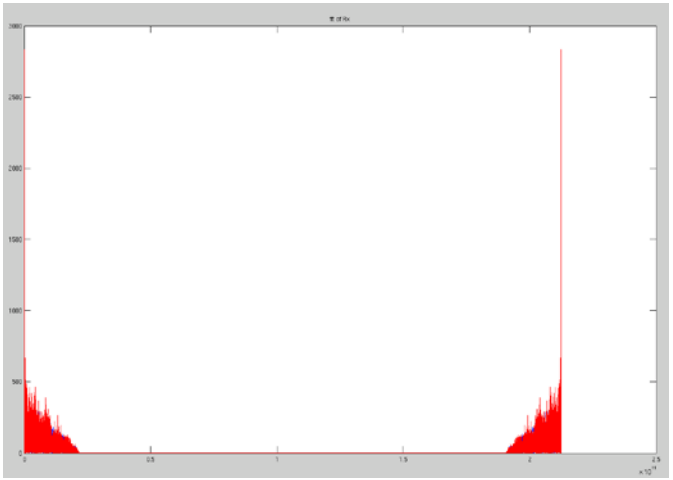
Electrical level distribution after EQ for SSPR pattern



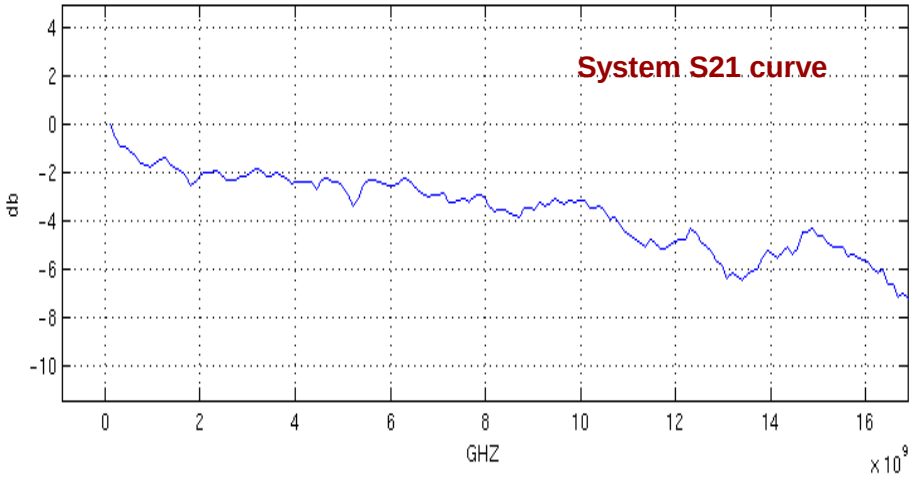
Further testing 56Gb/s PAM4, continued
Analysis of PRBS&SSPR in frequency domain



Spectrum of Tx(Blue: PRBS; Red: SSPR)

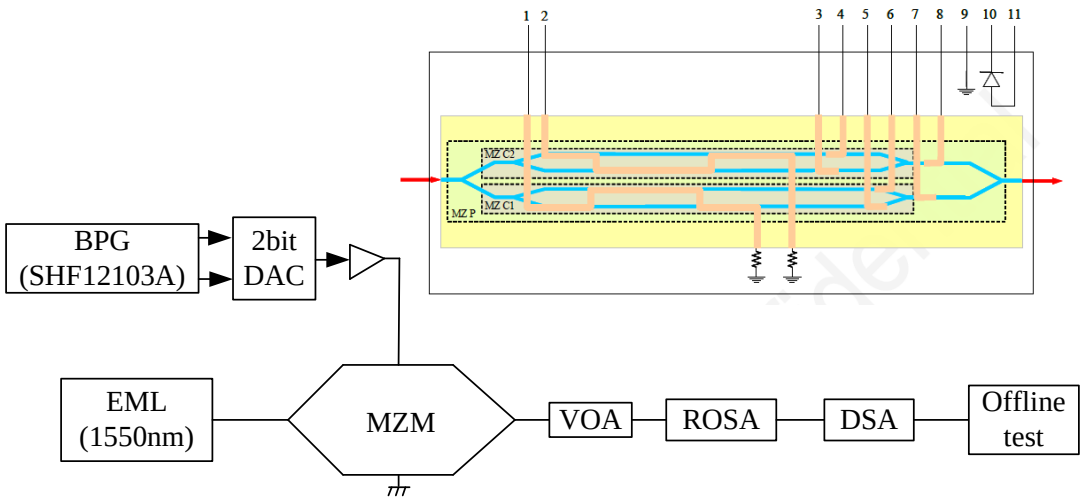


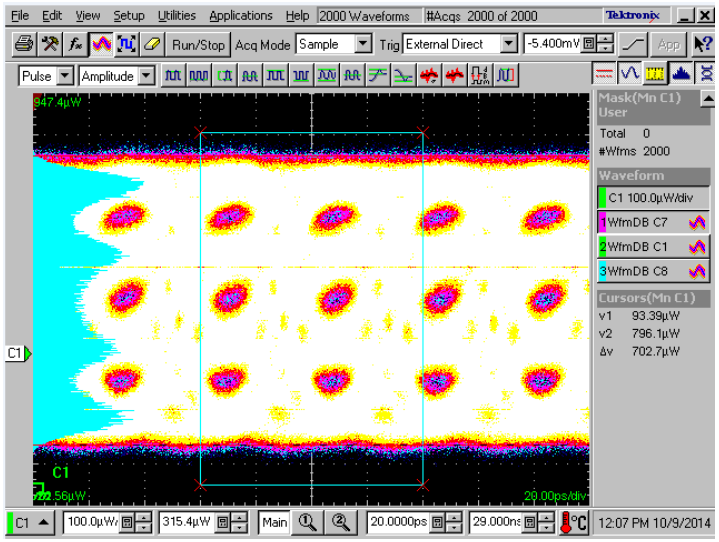
Spectrum of Rx(Blue: SSPR; Red: PRBS)



- **Comparing PRBS and SSPR pattern data in the frequency domain using FFT, we will see much stronger low frequency components in the SSPR signal (resulting from more long ‘0’ and long ’1’ combinations) with a peak around 3 MHz.**
- **From the system S21 (overall system transfer function) curve, the 3dB bandwidth is less than 12GHz.**

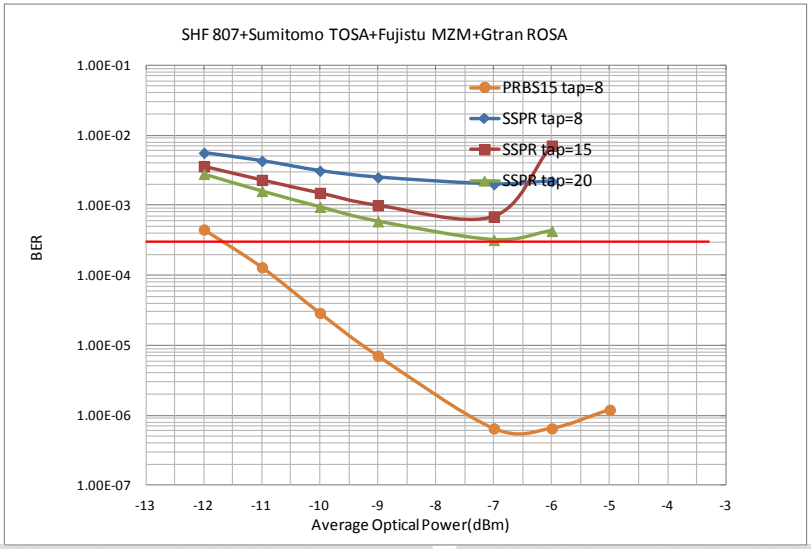
Further testing 56Gb/s PAM4, replacing EML with MZ





Optical eye diagram (AOP=-3.4dBm)

- Compared with EML, the optical eyes after MZ are more uniform, but with more narrow opening. Probably resulting from high linearity and low electrical bandwidth of used MZ
- The BER floor using the MZ modulator is lower than 1e-6 (6.5E-7) for PRBS15 pattern, but the BER floor for the SSPR pattern stays at 1e-4 level.



Required follow-up on checking BER performance

- We cannot rely to make decisions on single-data point test results with limited testing conditions like PRBS15, zero dispersion, zero jitter, etcetera.
- We need to confirm that a BER floor that close to the FEC operation point will stay where it is and not move strongly up/down for small variations of operating conditions.
- Therefore we will need to see more than one data-point on BER test results for all PMD proposals to ensure that we will be able to design practical 400Gb/s Ethernet systems that will have sufficiently robust BER performance under low-cost, high-volume manufacturing conditions

Further considerations on 4x100G PAM4 power budget

Recap of "stassar_01a_0914_smf", SMF Ad Hoc, 30 September 2014

	Realistic specification for 2km duplex SMF	Realistic specification for 500m PSM4 SMF	Unit
Tx OMA (01-00) min Specification Value	-5.5	-3.5	dBm
TDP	1	1	dB
Tx OMA (01-00) – TDP min	-6.5	-4.5	dBm
Wanted channel insertion loss, specification Value	4	4	dB
Rx ROP OMA (01-00) with KP4 FEC Specification Value	-6	-8	dBm
Available channel loss	-0.5	3.5	dB

For 2km duplex SMF the "gap" in this budget seems too big to be bridged. If reconfirmed then 4x100G PAM4 may only be useable for 500m PSM4.

Other view on 4x100G PAM4 power budget

Updated view on **realistic** numbers:

- Rx ROP OMA (01-00) -5 dBm instead of -6 dBm for 2km and 2 dB for PSM4
- TDP of 3dB instead of 1dB to calculate typical Tx power specification
- Bottom up calculation of needed Tx OMA specification for 4 dB channel loss

	Realistic specification for 2km duplex SMF	Realistic specification for 500m PSM4 SMF	Unit
Tx average, Before Mux	+6	+4	dBm
Tx OMA (01-00), Before Mux	+4	+2	dBm
Tx OMA (01-00) min	+2	0	dBm
TDP	3	3	dB
Tx OMA (01-00) – TDP min	-1	-3	dBm
Channel insertion loss	4	4	dB
Rx ROP OMA (01-00) with KP4 FEC Specification Value	-5	-7	dBm

Can we do average Transmitter output powers of +6 or +4 dBm?

Summary

- Further test results and considerations on error floor performance in PAM4 experiments have been provided.
- Suggestions for necessary follow-up to provide extensive additional test results have been made .
- An updated view (from stassar_01_0914_smf) on potential power budgets for 4x100G PAM4 has been given.
- Maintaining the view, that 50G per λ, either NRZ or PAM4, as presented in stassar_3bs_01b_0914, is still the proposed direction for 802.3bs.

Q & A

Suggested to continue by offline debate and SMF Ad Hocs

Thank you