56GBaud PAM4 Error Floor Analysis

Alan Tipper Nov 2014

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  - Francois Tremblay, Semtech

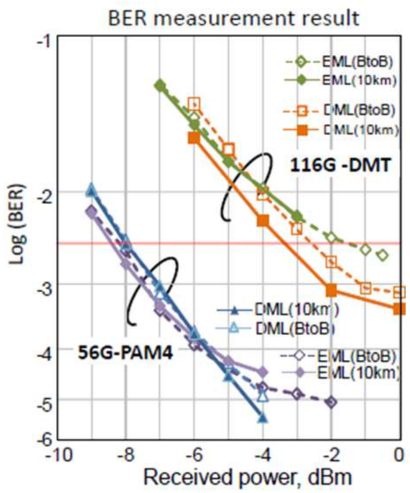
The Demise of the Waterfall Curve?

- Gaussian BER waterfall curves ~0.5erfc(Q/√2) from old NRZ systems require that noise and signal be independent and are not applicable to systems with significant signal:noise correlation
- High bandwidth multilevel systems are more complex
  - Source RIN is significant and is signal dependant
  - Shot noise can't be ignored and is signal dependant
  - Sampling ADC has a finite noise floor relative to the full scale range so is signal dependant once AGC is used
  - Tx DACs have finite SNR/ENoB
  - Other secondary effects that may not be equalized out
    - Residual nonlinearity, chromatic dispersion, long impulse reflections
- FEC has to be used to guarantee acceptable BER
- Telco systems successfully operate with low Raw BERs today
  - DWDM systems have OSNR limited raw error floors
  - Coherent systems operate with EVM limited raw error floors
  - WiFi, 3G Cellular operate with error floors from multipath
- In a mandatory FEC environment a monotonic raw error rate is no longer essential
  - **We just need to understand and bound the raw error rate** to ensure we meet the post FEC performance criteria.

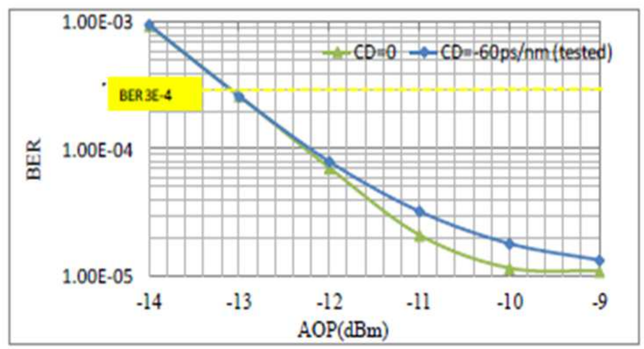
Part 1: Understanding the Experimental Error Floors

Recap: Error Floors observed on all PAM4 Experiments at 28 & 56 GBd (Full list in Appendix)

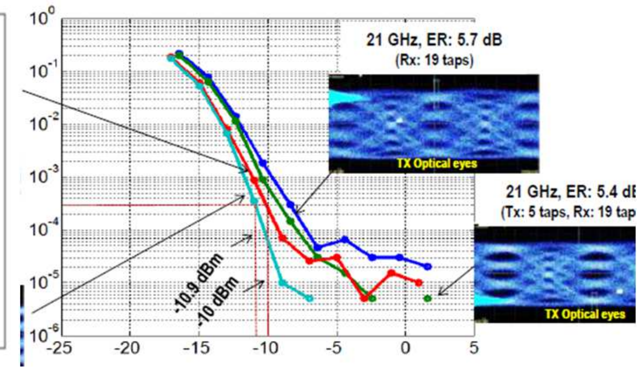
28GB



Sone_3bs_01_0914

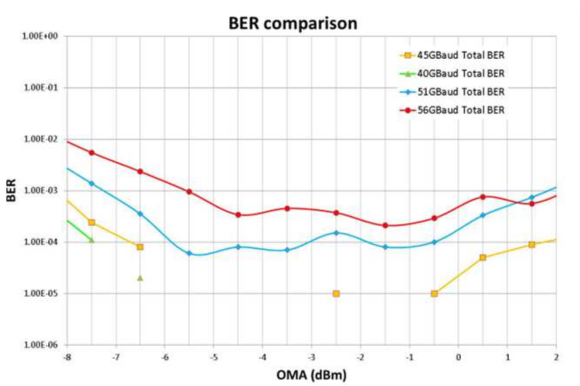


xu_3bs_01_0714

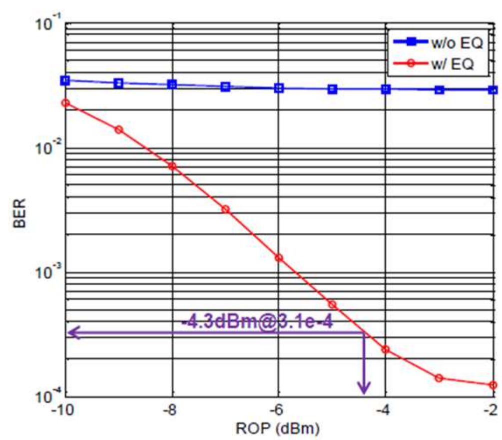


way_3bs_01a_0514

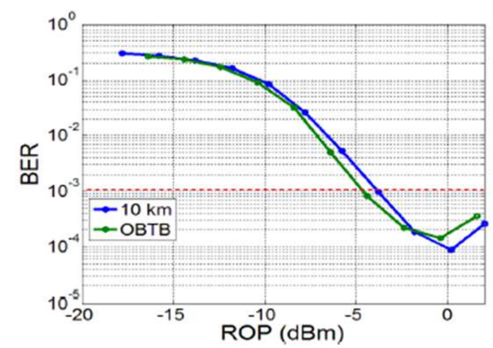
56GBd



Mazzini_3bs_01_0914



Song_3bs_01a_0514

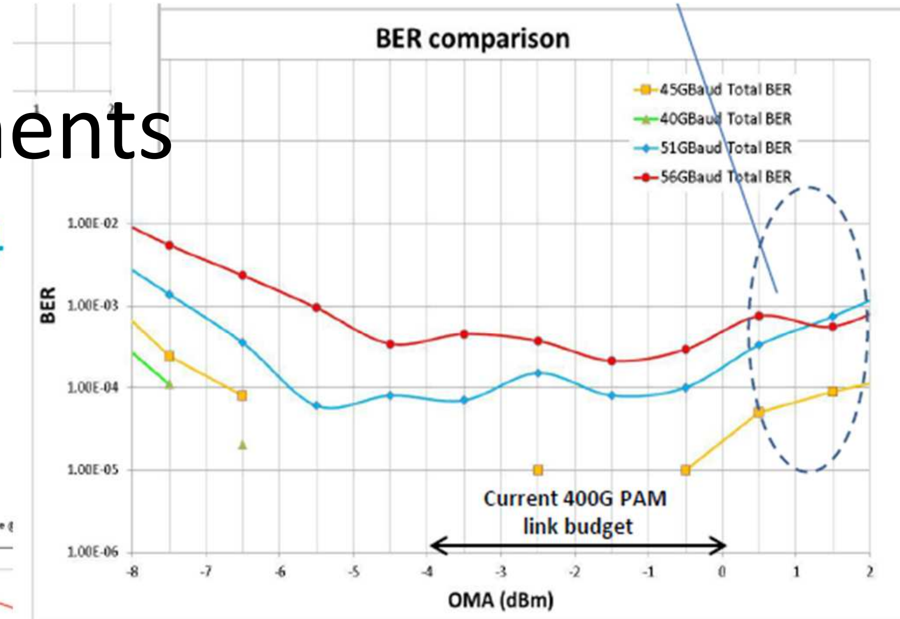


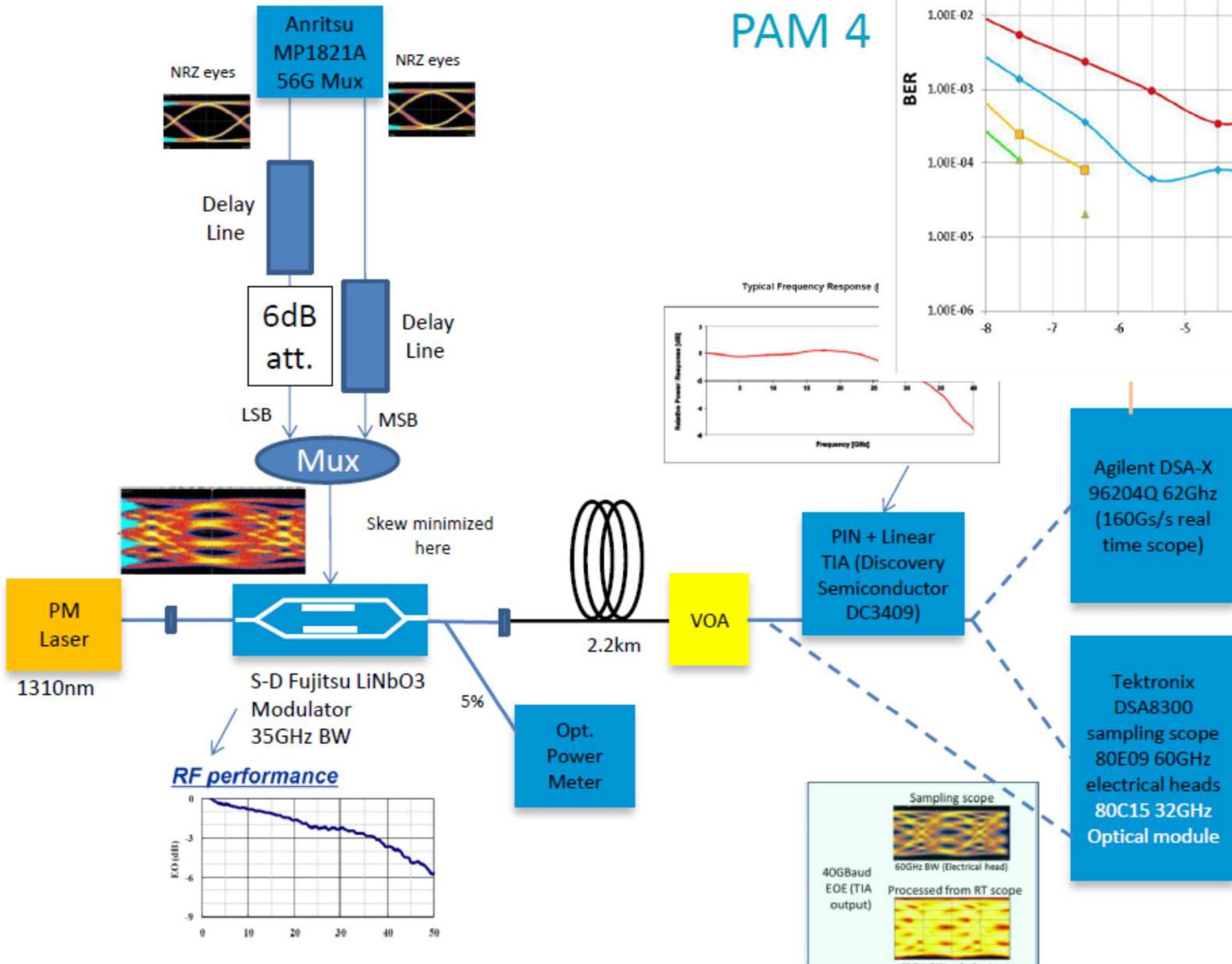
way_3bs_01a_0914

Some Clues

- Stassar_3bs_01_0714
  - Noted that improving cables and lowering ADC noise improved 56Gbaud floor from 1E-4 in Song_3bs_01a_0514 to 2E-5 so ADC noise might be a contributor to the floor.
- Xu_3bs_01a_0514
  - Noted that TX SNR did not have a strong effect on sensitivity at 28Gbd although did not explore the error floor. However comparison of 2 different EA drivers (with different SNRs) shows error free & 1E-6 at the electrical output (i.e before the EA) stage so driver SNR might be a contributor to the floor.
  - MPI noted to produce a sensitivity penalty but does not significantly degrade the error floors in a 28GBd experiment.

Example: Cisco Experiments





Source: Mazzini_01a_0814

Raw captured data files supplied by Cisco for this analysis.

Optical input range -10dBm to +2dBm
In 1dB steps.
262144 samples per capture @160GSa/s
91,840 symbols duration
PRBS15 pattern
T/2 spaced FFE EQ

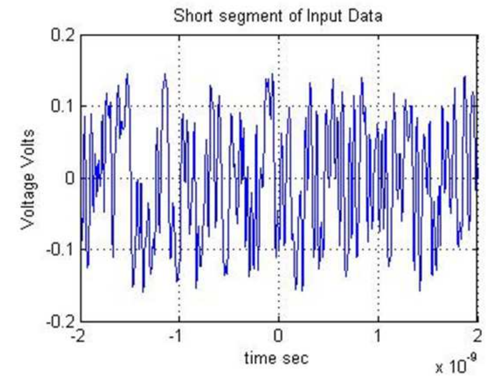
We need to understand the root cause of the experimental error floors seen on 56GBd PAM4 demonstrations

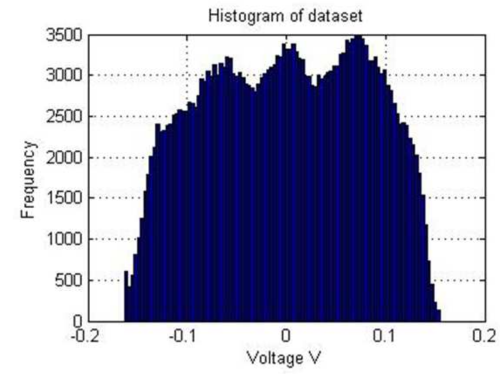
Matlab Post-Processing of Cisco Measurements

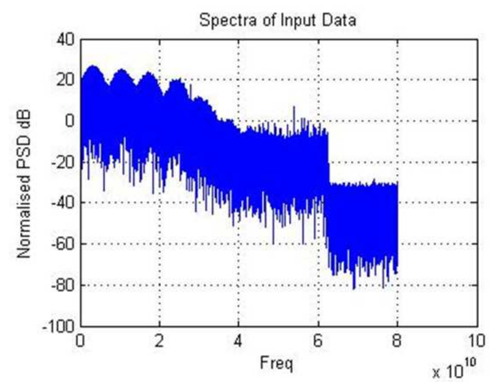
- Low ADC Enob?
  - Noise reduction filter added with Fc=35GHz
    - No improvement in BER
  - Reduce optical input by 3dB
    - No change in post FFE signal/noise ratio
  - **ITS NOT THE ADC NOISE FLOOR**
- Test Bench Reflections?
  - Autocorrelation ‘feature’
    - 140psec peak may be from PRBS delay
  - Extend FFE well beyond the ‘feature’
  - No improvement in BER with 100 taps
  - No autocorr 2nd peak on NeoPhotonics * data
  - **IT’S NOT ELECTRICAL REFLECTIONS**
- Patterning in the Post FFE data?
  - Look for pattern position dependant errors
  - Errors are well distributed across the pattern
  - More errors in the upper eye
  - **IT’S NOT PATTERNING**

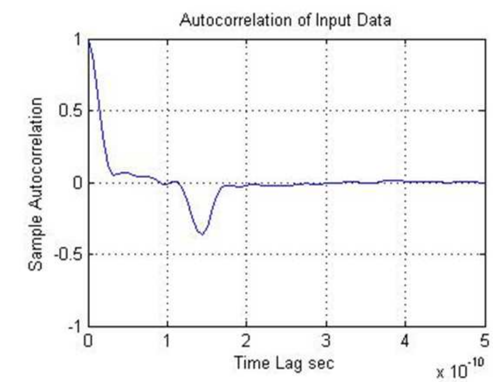
The BER floor does not appear to be a deterministic/ISI issue

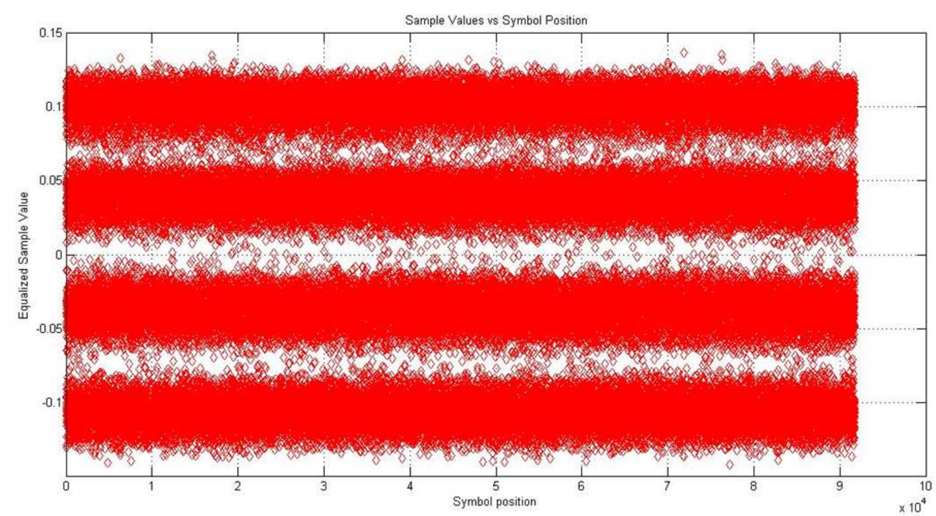
* 2nd set of Raw data from Way_3bs_01a_0914





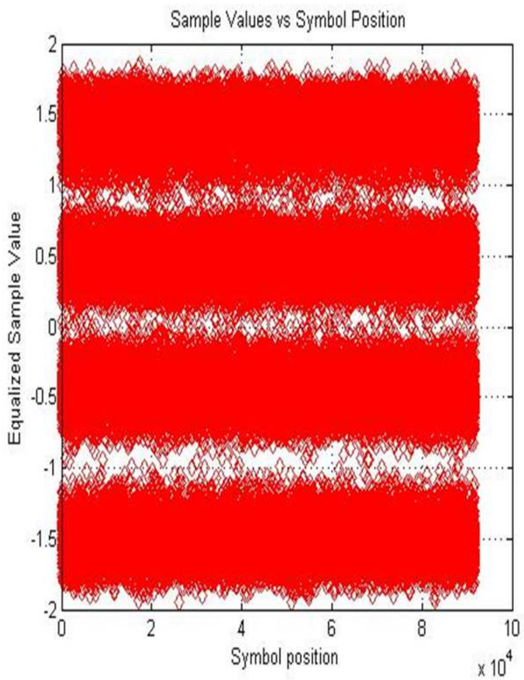


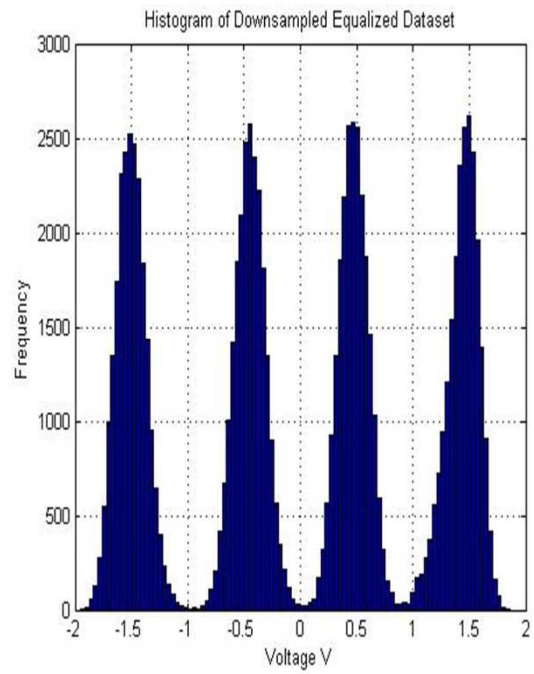




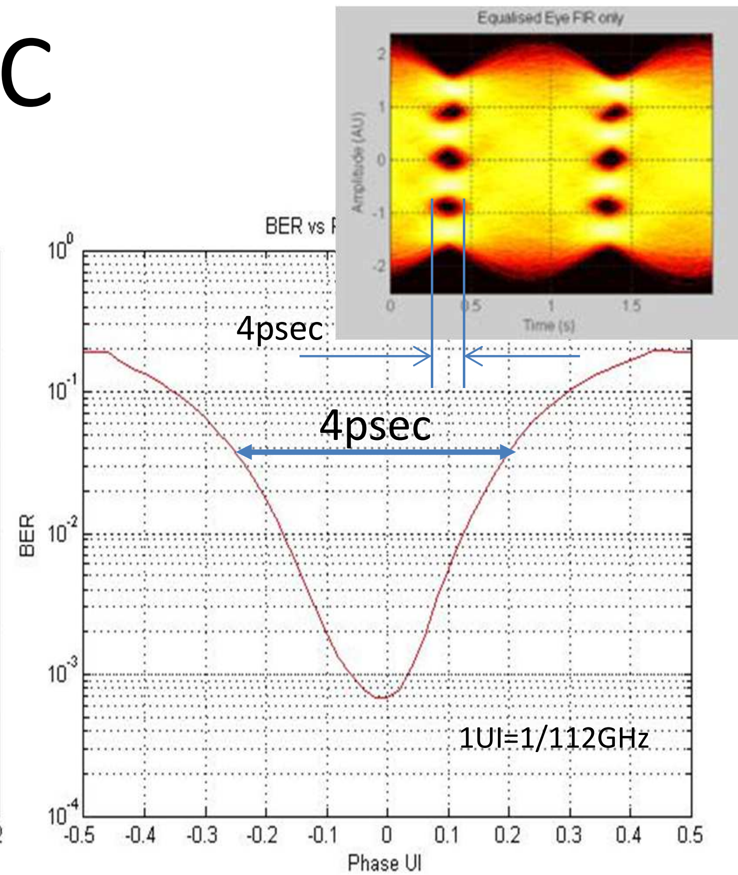
Post FFE recovered samples

70 TAP FFE, 35GHz Brickwall Noise Filter after ADC





Mazzini 22Tap EQ Measurement



Background BER improves slightly to 7E-4
(Noise Filter & Long FFE do not make much difference)

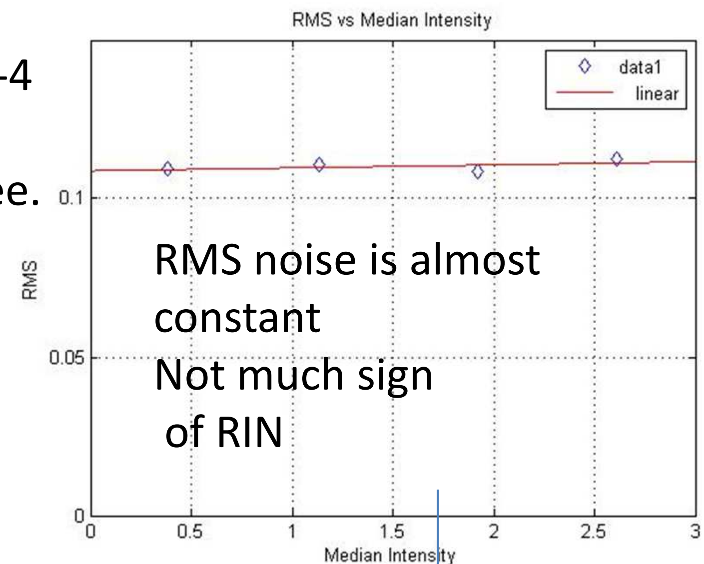
BER vs sampling phase for the T/2 Equalizer. Tap weights kept constant as sampling phase adjusted. 0dBm data set.
(Tx driver jitter ~ 6ps pk-pk#)
Sampling jitter ~190fs RMS*

*Sampling jitter from Agilent 96204Q spec sheet
Driver jitter estimated from Anritsu 1821A data

What can we deduce about the Noise?

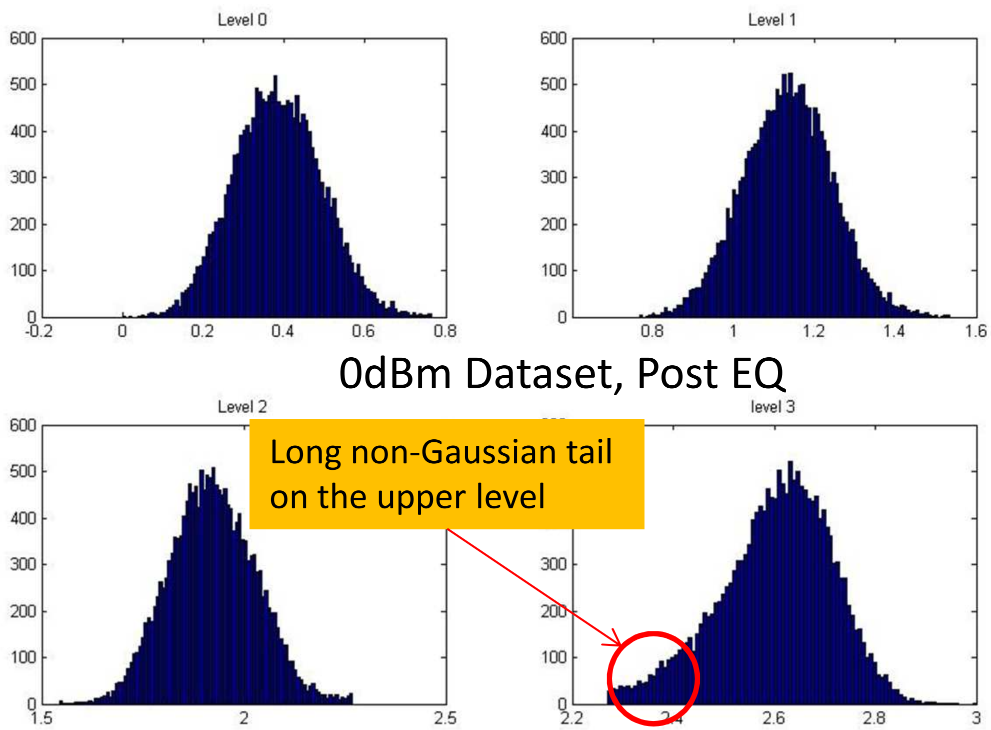
With RMS=0.11 and signal pk-pk=2.285 (0-3) we would expect an ideal BER=(3/8)*erfc(2.285/0.11/6/1.414) = 2E-4

Given the long tail noted below this is close to what we see. We would expect an error floor around 2E-4 even without the long tail.

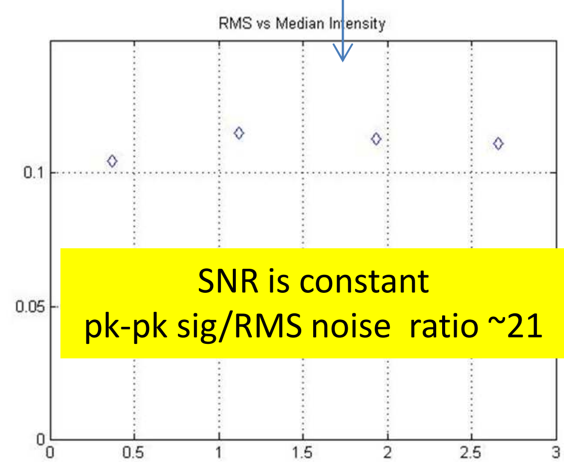


Reduce input By 3dB

Scale for Constant Vpk-pk (AGC)



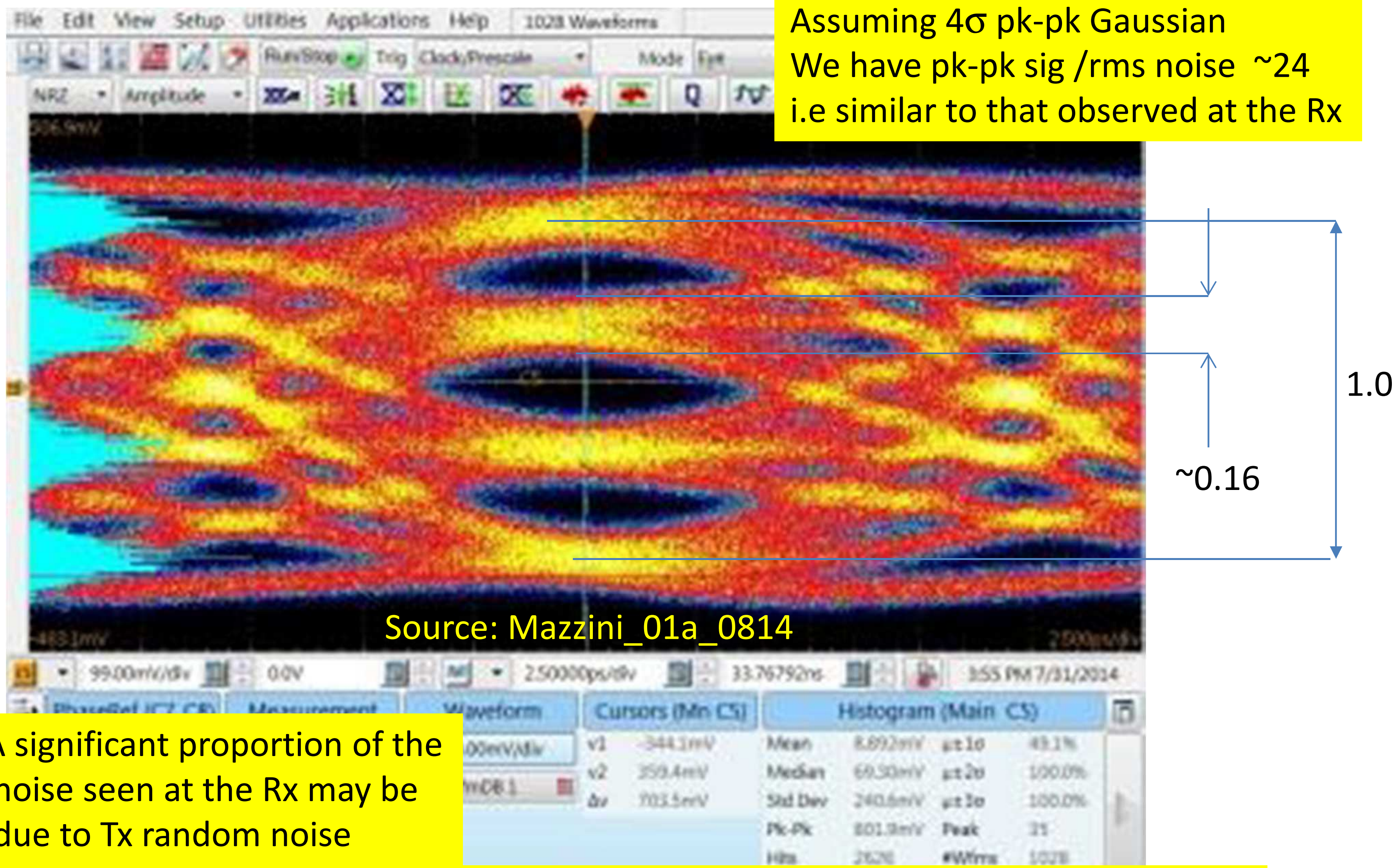
0dBm Dataset, Post EQ



The most likely causes of constant SNR are ADC Enob (already excluded) or TX SNR.

TX SNR Recap – Electrical Drive

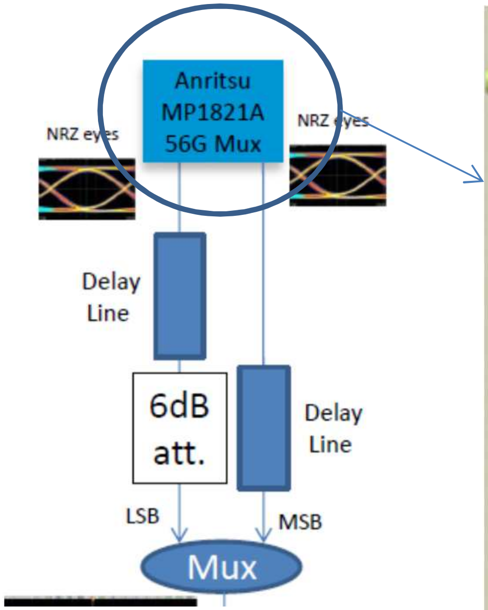
Assuming 4σ pk-pk Gaussian
We have pk-pk sig /rms noise ~24
i.e similar to that observed at the Rx



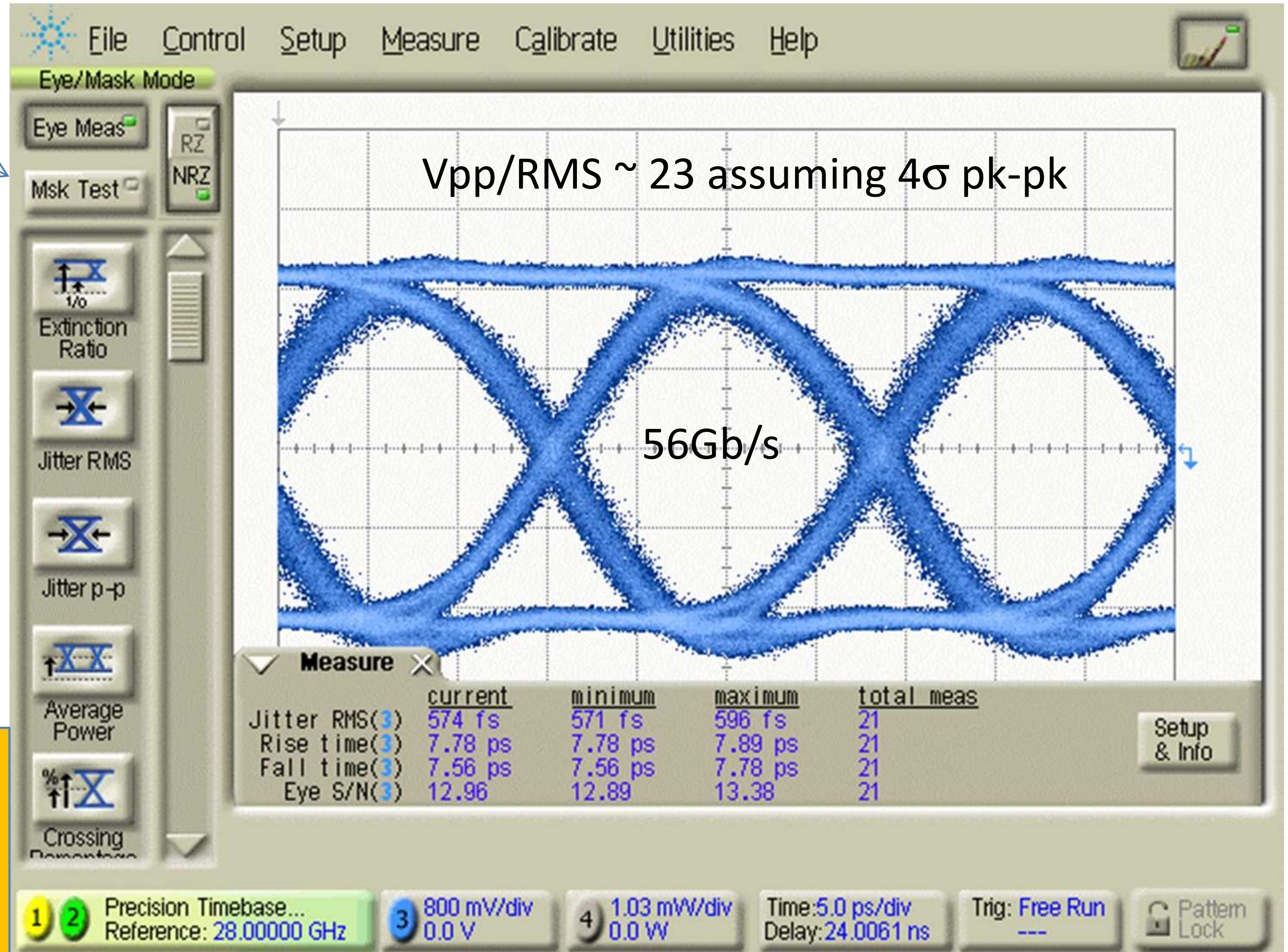
A significant proportion of the noise seen at the Rx may be due to Tx random noise

What we don't know is how much is random (non-equalizable) and how much is ISI

Anritsu MP1821A 56G MUX Used in Experiment



Source: Mazzini_01a_0814



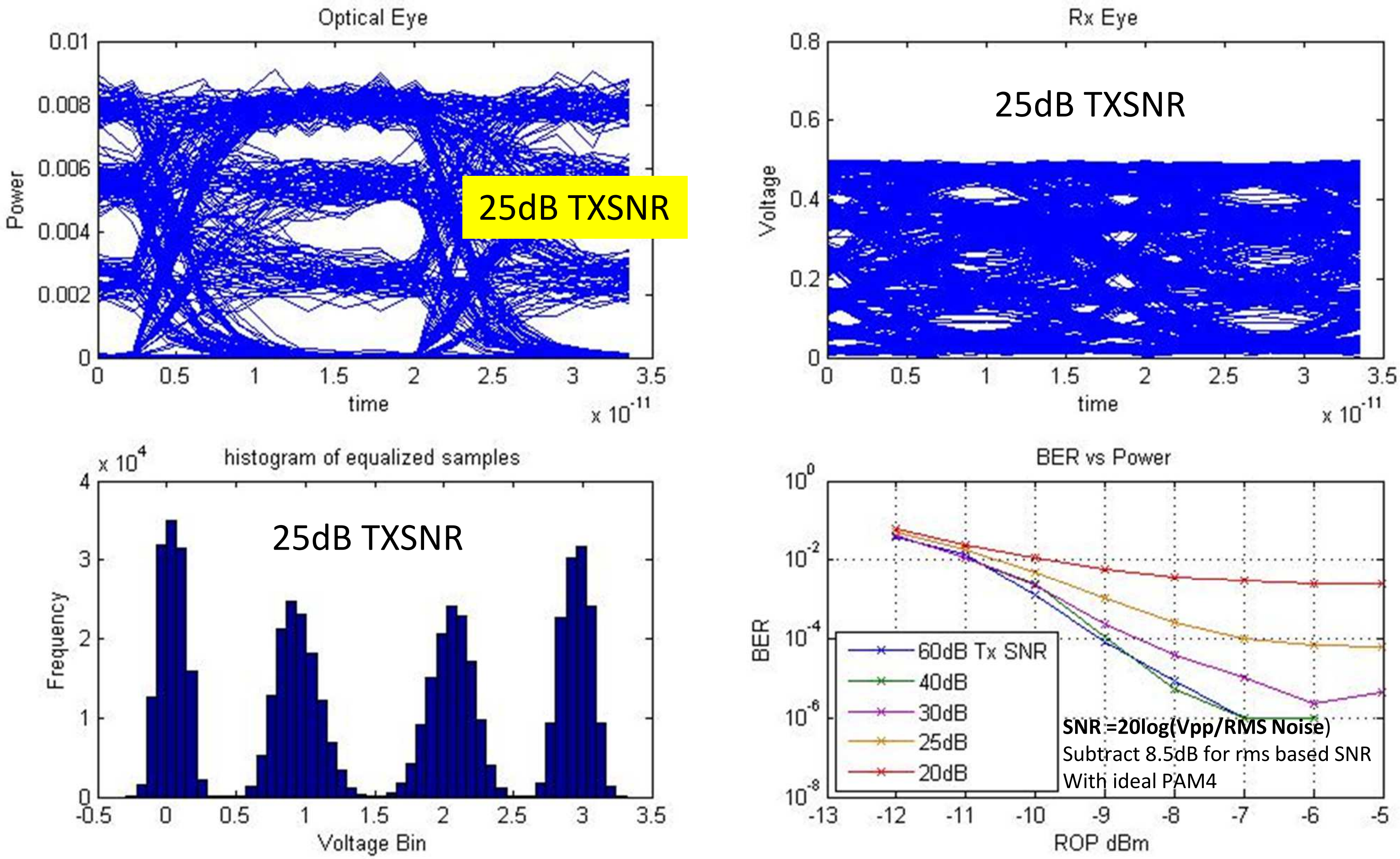
Source: MP1821A22A_56G_EL2100.pdf available from Anritsu website

Once the two outputs are summed to generate a PAM4 signal The pk-pk/RMS will be <23 i.e comparable to the noise seen at the Rx on each level

Adequate SNR for NRZ Instrumentation is problematic for PAM

If it’s Tx SNR, does it pass the Simulation test?

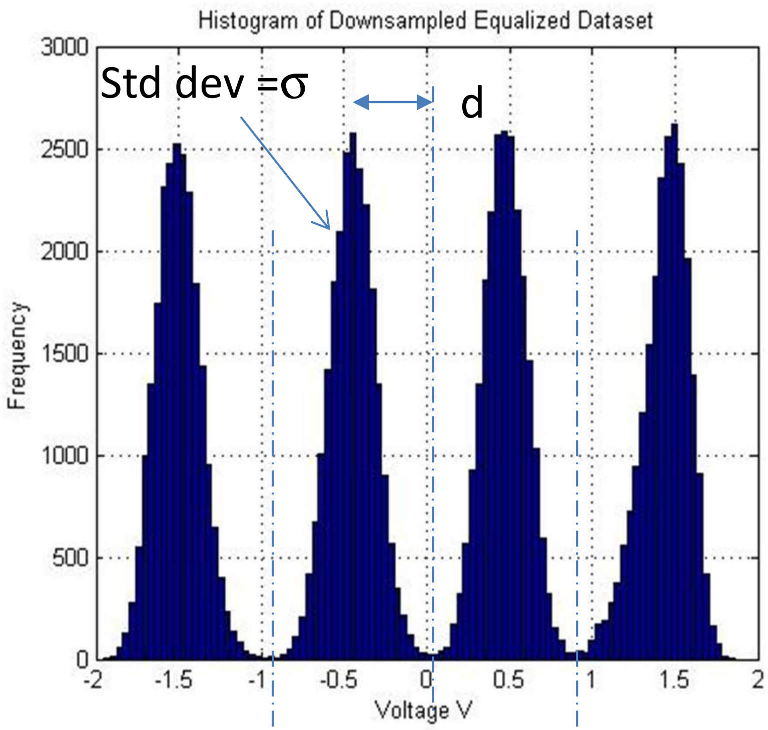
R=0.6A/W 23pA/rt Hz 30GHz Rx BW -140dB/Hz RIN 6ps/nm.km CD
0.5ps/rt km PMD 2km SMF ADC Enob=5 5% Rx THD TX **SNR =20log(Vpp/RMS Noise)** at driver o/p



Simulation replicates the error flooring mechanism and the histogram closure

Part 2: Bounding the Error Floors

Contributors to the BER



Measured Histogram of Post Equalization Samples
(Source: post processed from Mazzini_01a_0814)

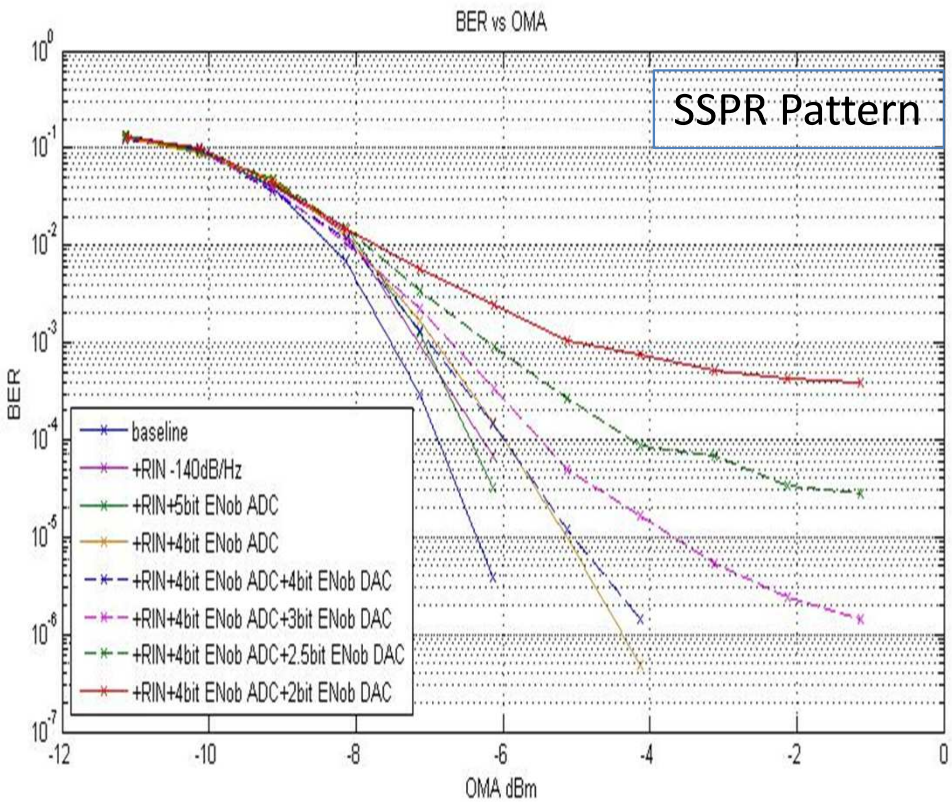
- The 'd' terms
  - Pk-Pk photocurrent
  - Unequalized ISI
    - Chromatic Dispersion
    - Nonlinearity
    - Data/clock Alignment jitter
- The 'σ' terms (*italic* terms are correlated with d)
  - TX Random noise
    - *Laser RIN*
    - *Driver/DAC random noise*
  - Path random Noise
    - *MPI*
  - RX Random noise
    - *Detector shot Noise*
    - TIA Noise
    - *ADC random noise*
    - Equalizer noise Enhancement

Theoretical Ideal: $BER = \frac{3}{8}\text{erfc}(\frac{d}{2\sqrt{2}\sigma})$

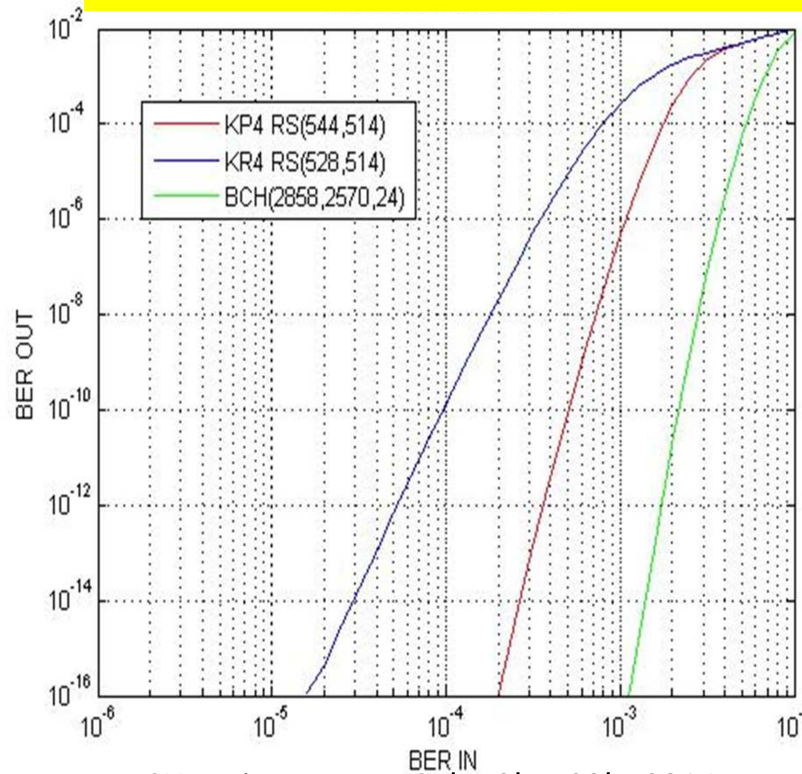
Assumes d,σ uncorrelated, uniform levels Gaussian noise

When $\frac{d}{\sigma} \rightarrow$ Constant we get an error floor

56Gbd Matlab Simulation



Corrected BER plots for KP4,KR4 & BCH FEC (random errors)



BCH variant as per Cole_3bs_02b_0914

Baseline: 23pA/rt Hz TIA, 0.6A/W, 30GHz Rx BW, 5% RX THD, 6psec/nm.km CD, 0.5psec/rt km PMD,2km SMF, 7 tap T spaced FFE, Gray coded data, MZI transmitter 5% THD driver.

For analogue Tx convert DAC Enob to pp/rms SNR using:
20log(Vpp/rms noise)=6.02ENoB+1.76+9 dB

Recommendation for raw error floors < 10^{-6} and corrected BER < 10^{-15} is
ADC ENob>5 and DAC Enob>4 (Other trade offs ok with nonlinearity & RIN but a good starting point)

Summary

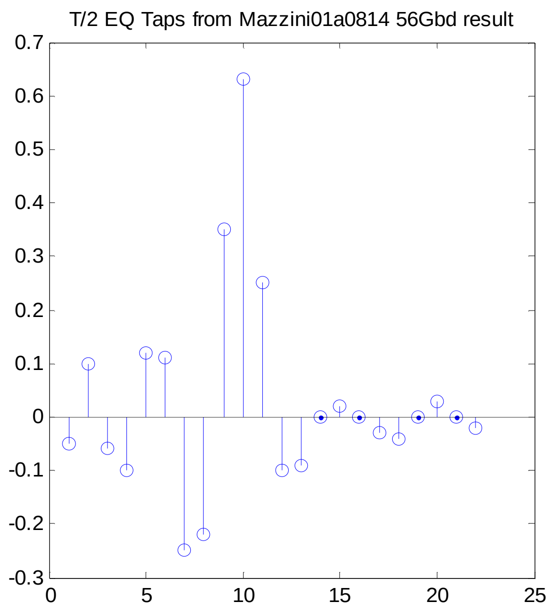
- For FEC mandated systems, monotonic raw error rates are not essential and many systems operate today without that.
- Lab measurements using discrete components are clearly sub optimal due to all of the interfaces and low bandwidth end to end.
- Reference Transmitters intended for NRZ applications may have insufficient SNR for realistic PAM4 experiments.
- Raw Error floors are predicted by theory and can be addressed by:
  - Budgeting for Tx as well as Rx SNR
  - Ensuring an ADC Enob > 5
  - Ensuring Tx Driver SNR > 35dB (defined as 20log[Vpp/RMS]) or DAC ENoB>4
  - Minimizing non equalizable ISI by careful design
    - (particularly cables, reflections, nonlinearity)
  - Not relying on the EQ to cure all H/W ills
    - Too much EQ causes noise enhancement
    - Better analogue hardware will yield lower error floors
- Target ADC & DAC ENoB values are consistent with FEC corrected error rate floors $<10^{-15}$

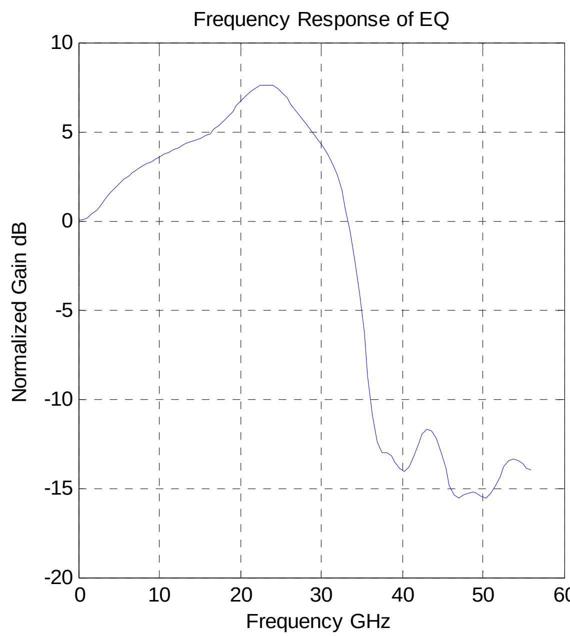
Appendix

14 Experimental PAM Results so far

- Stassar_01_1014_smf
- Sone_3bs_01_0914
- Mazzini_3bs_01_0914
- Way_3bs_01a_0914
- Stassar_3bs_01_0714
- Xu_3bs_01_0714
- Bhatt_3bs_01a_0714
- Hirai_3bs_01a_0714
- Shirao_3bs_01a_0714
- Hirai_3bs_01_0514
- Song_3bs_01a_0514
- Xu_3bs_01a_0514
- Bhoja_3bs_01_0514
- Way_3bs_01a_0514

High Pass Response of EQ will Enhance Noise





A linear equalizer will minimize ISI but the resulting High pass response will degrade Random noise

$$NEF = \sqrt{\frac{\int |H(f)|^2 df}{Fbaud/2}} = 1.24$$

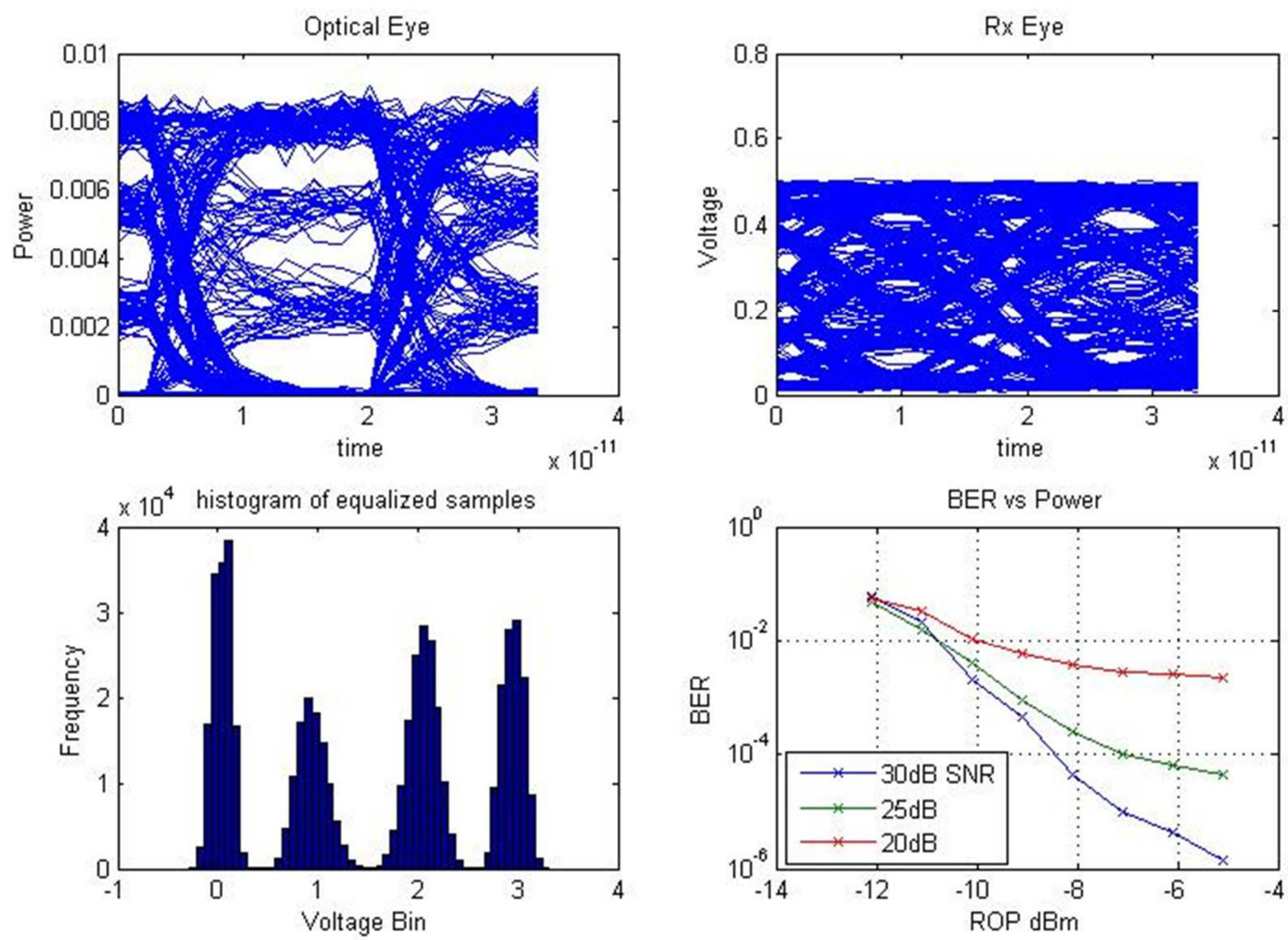
EQ gain of ~7dB at 23GHz indicates that
The end-end channel bandwidth was very low
In that experiment!

Estimated using a brickwall 0.5 x baudrate filter as the baseline

Raw data from Mazzini_01a_0814, used to determine typical values and assumed applicable to other experimental work.

Repeating the TXSNR Simulation with SSPR Rather than PRBS 15

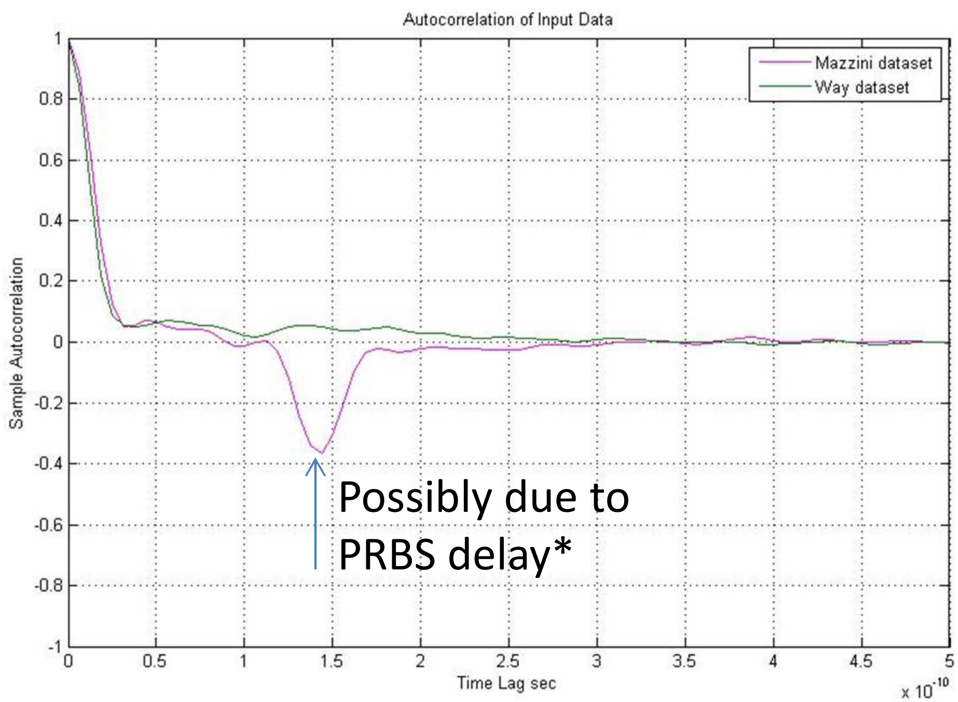
(other simulation parameters unchanged)

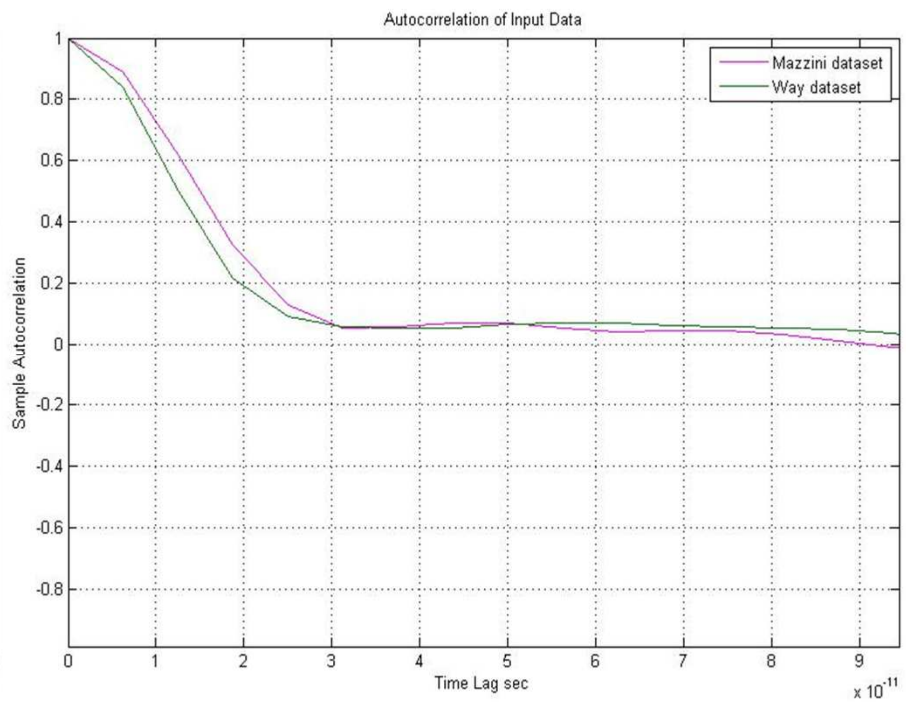


Not significantly different from PRBS result.

Datapath Reflections?

Mazzini_3bs_01_0914 & Way_3bs_01a_0914 Datasets compared





*Pattern matching of the MSB/LSB content to PRBS in the Mazzini data shows the two streams to be delayed by 8 symbols i.e 143psec.
Way dataset generated PAM from a multilevel random generator in software so no delays