
Error Floor Investigation for both 56 and 112Gb/s PAM4 Signals

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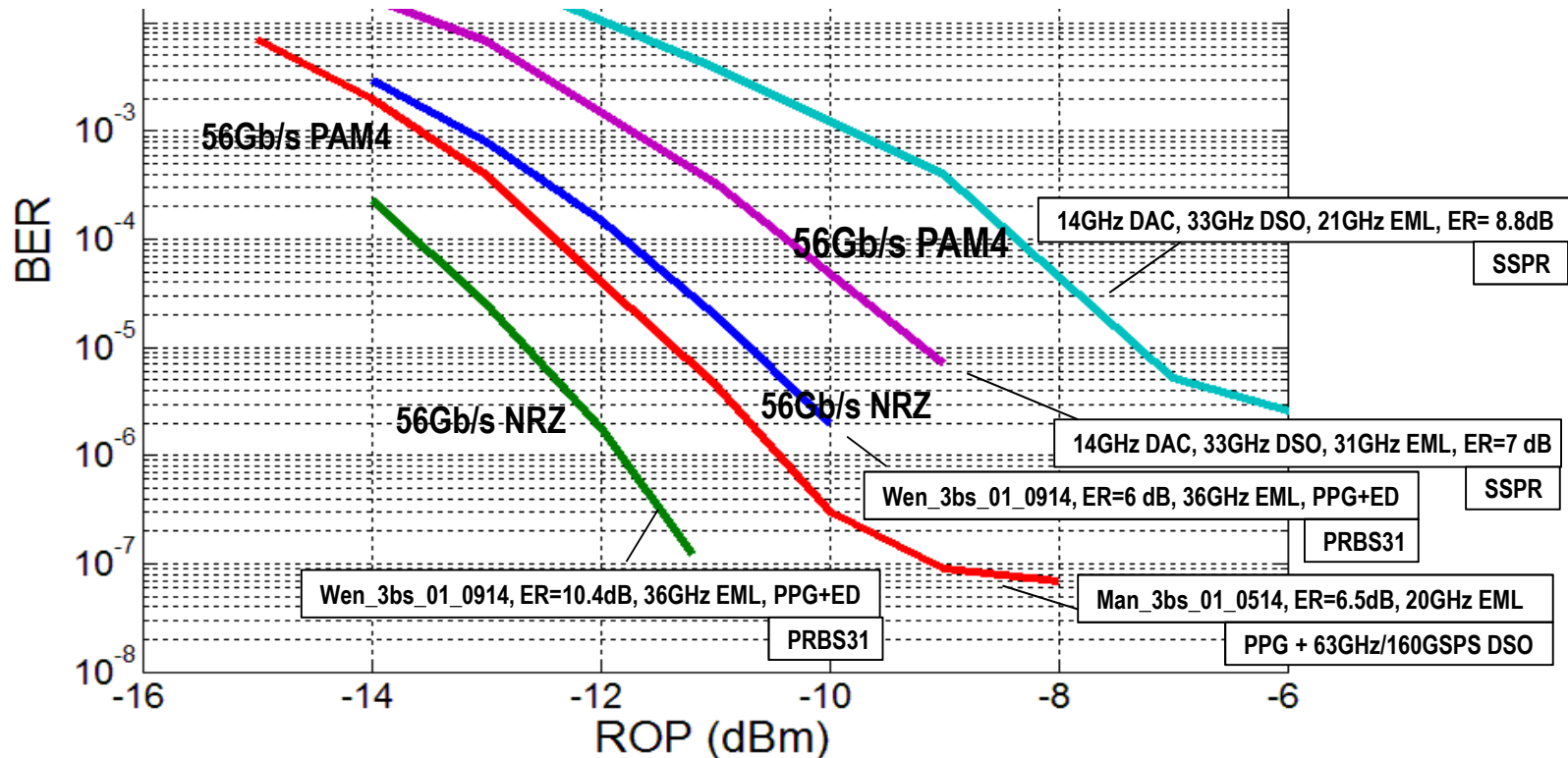
Goal

- Carry out end-to-end system simulation to investigate the main root causes of bit-error floor in 56Gb/s and 112Gb/s PAM4 links by using a practical number of FFE taps, and by using existing optical transmitters, receivers, and driver amplifiers.
- Simulation confidence-level is established via matching with our previous experimental results.

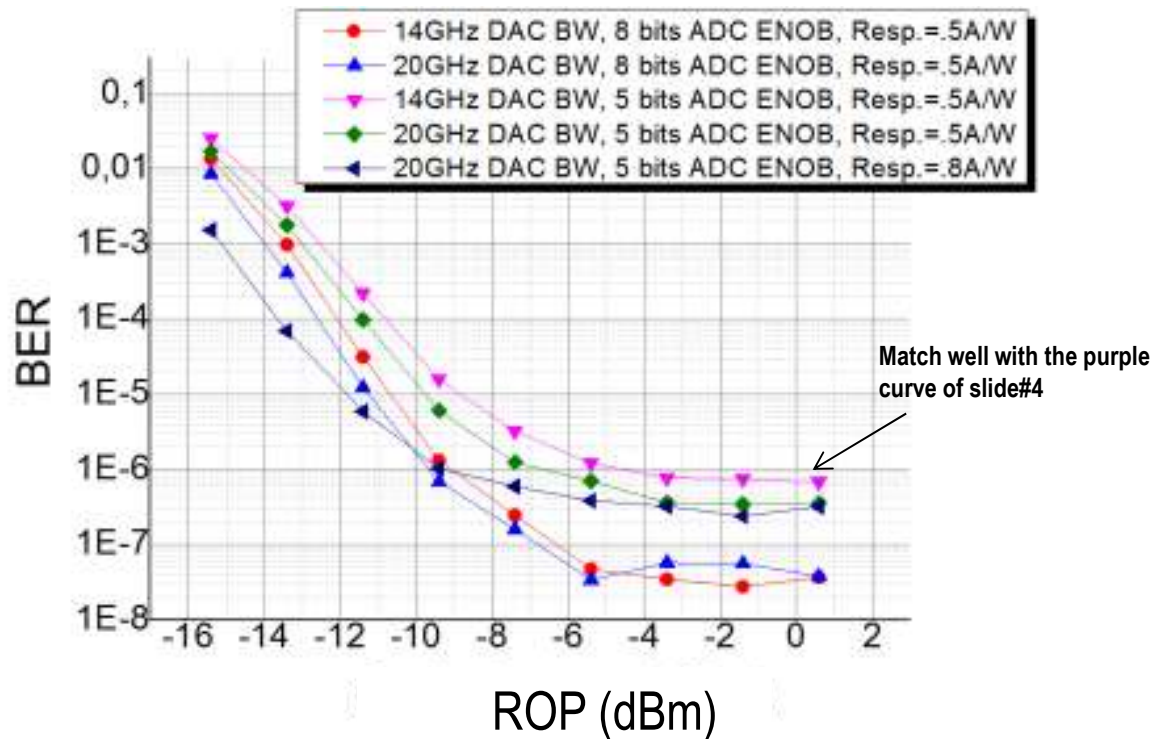
56Gb/s PAM4

Comparing 56Gb/s PAM4 with NRZ- experimental data

1. 56Gb/s PAM4 can out perform NRZ if DAC and ADC bandwidth & ENOB limitations are essentially removed, and can use 20GHz EML as opposed to NRZ's 36GHz EML .
2. Even with limited DAC and ADC bandwidth & ENOBs, error floor can occur at a low BER~ 1e-6



Error Floor (at BER <math> < 1e-6 </math>) cause 1 : DAC analog BW limitation and ADC ENOB



Electrical SNR before a 31GHz EML is 21dB
ADC bandwidth= 25GHz

Baud rate= 28Gbaud

Driver amp BW=31GHz

SNR before EML = 21dB

ER = 9dB (31GHz EML)

WL=1310nm

RIN=-145dB/Hz

10km SSMF

RX input noise density=17pA/ $\sqrt{\text{Hz}}$

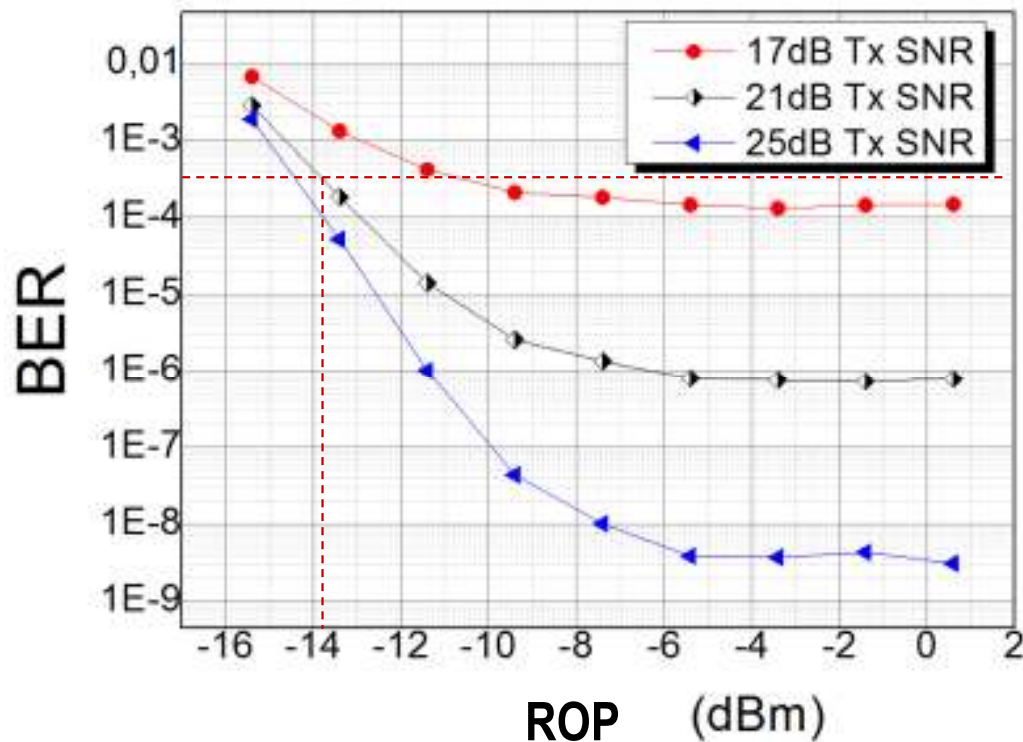
PD+ linear TIA BW=22GHz

1st-order Bessel approximation of EML,
DAC, PD+TIA, driver amp.

5th-order Bessel approximation for
ADC

21-tap T-spaced FFE

Error Floor cause 2: Electrical SNR before E/O (DAC ENOB & driver related)



Baud rate= 28Gbaud

Driver amp BW=31GHz

ER= 9dB (31 GHz EML)

WL=1310nm

RIN= - 145dB/Hz

10km SSMF

RX input noise density= 17pA/ $\sqrt{\text{Hz}}$

PD+ linear TIA BW=22GHz

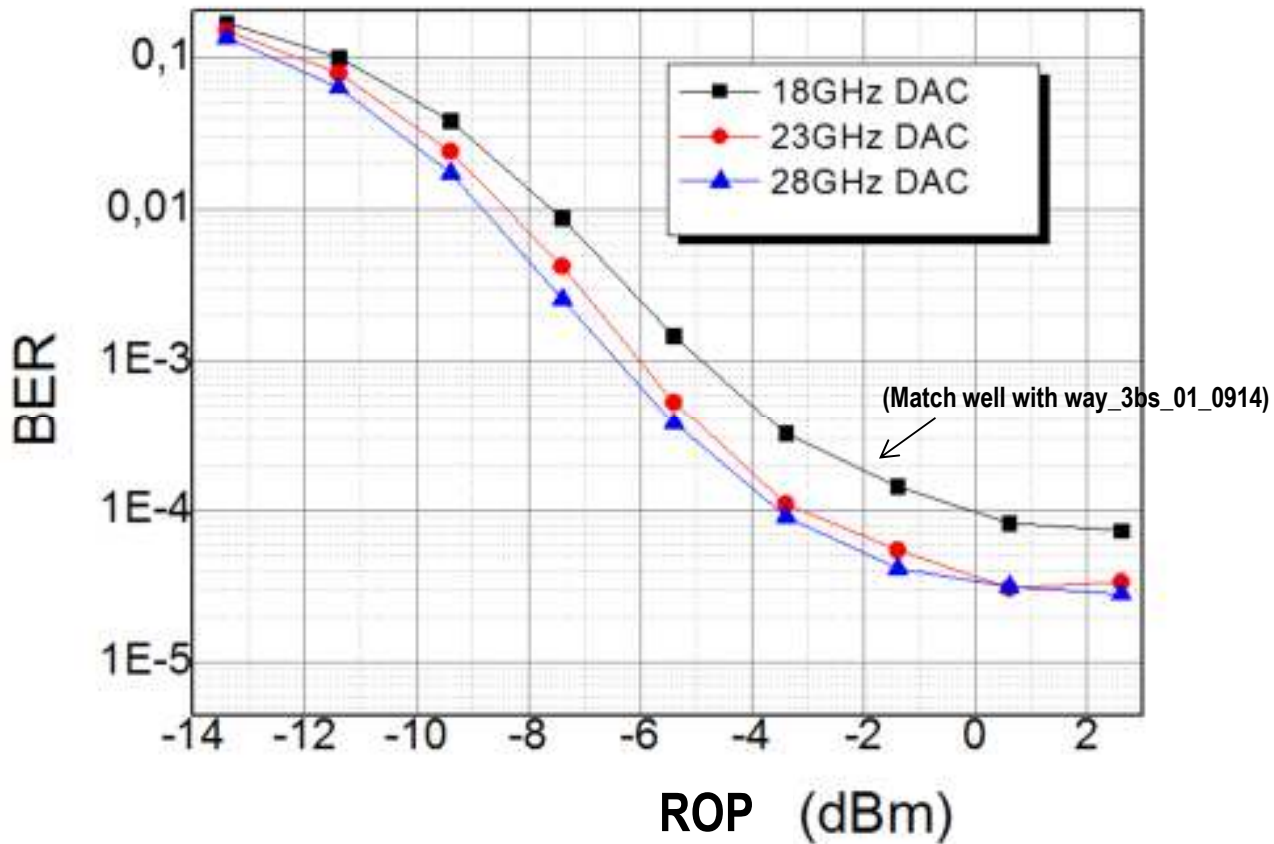
0.8A/W responsivity

21-tap T-spaced FFE

(DAC bandwidth= 14GHz)
(ADC bandwidth= 25GHz, ENOB= 5)

112Gb/s PAM4

112Gb/s PAM4 DAC BW Effects



(ADC bandwidth= 63GHz, ENOB= 5)

Baud rate= 56Gbaud

TX Driver AMP BW=31GHz

SNR before EML = 21dB

EML BW=32GHz

Optimized modulation index

WL=1310nm

RIN=-145dB/Hz

10km SSMF

RX input noise density= 40 pA/ $\sqrt{\text{Hz}}$

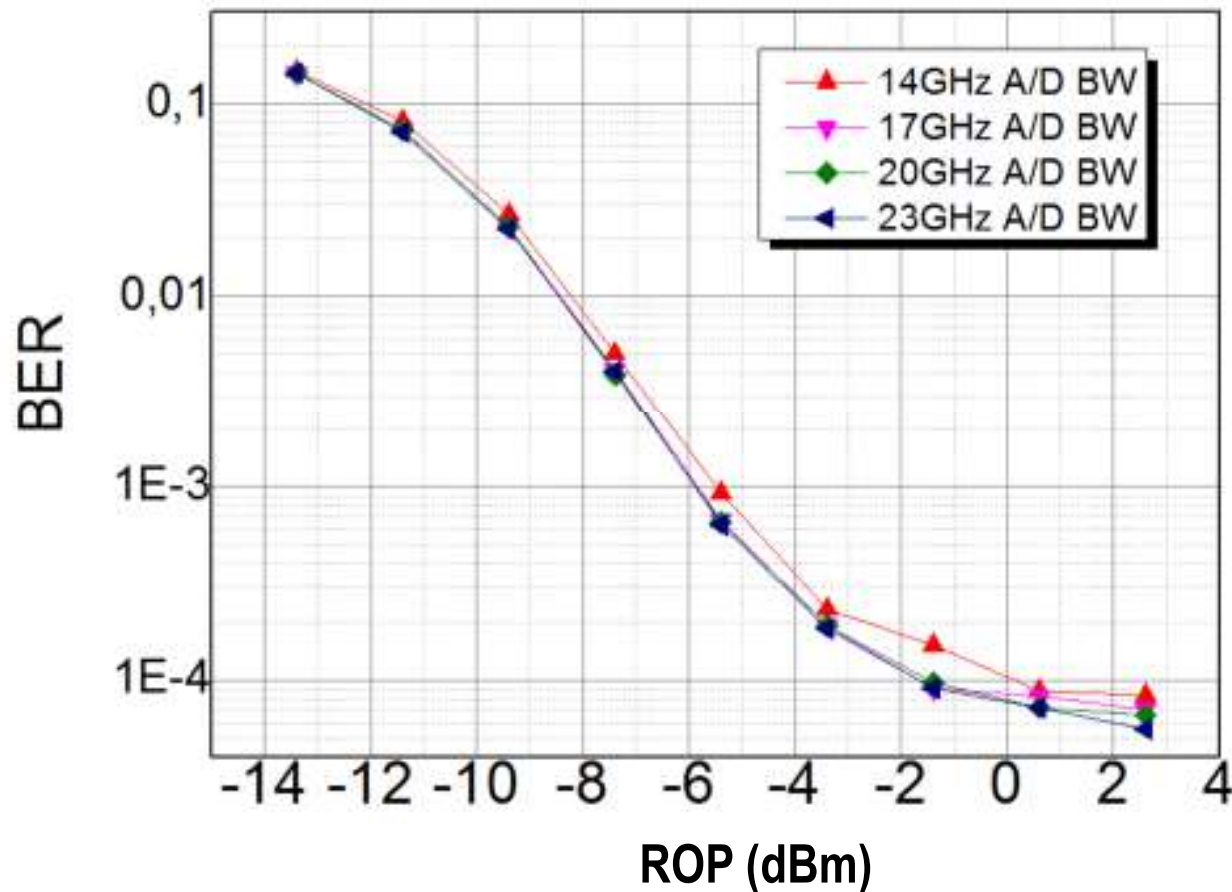
PD+ linear TIA BW= 40GHz

21-tap T-spaced FFE

1st-order Bessel approximation of E/O and PD+TIA

5th-order Bessel approximation for ADC

112Gb/s PAM4 ADC BW Effects



(DAC bandwidth= 23GHz)

Baud rate= 56Gbaud

TX Driver AMP BW=31GHz

SNR before EML=21dB

EML BW=32GHz

Optimized modulation index

WL=1310nm

RIN=-145dB/Hz

10km SSMF

RX input noise density=40 pA/ $\sqrt{\text{Hz}}$

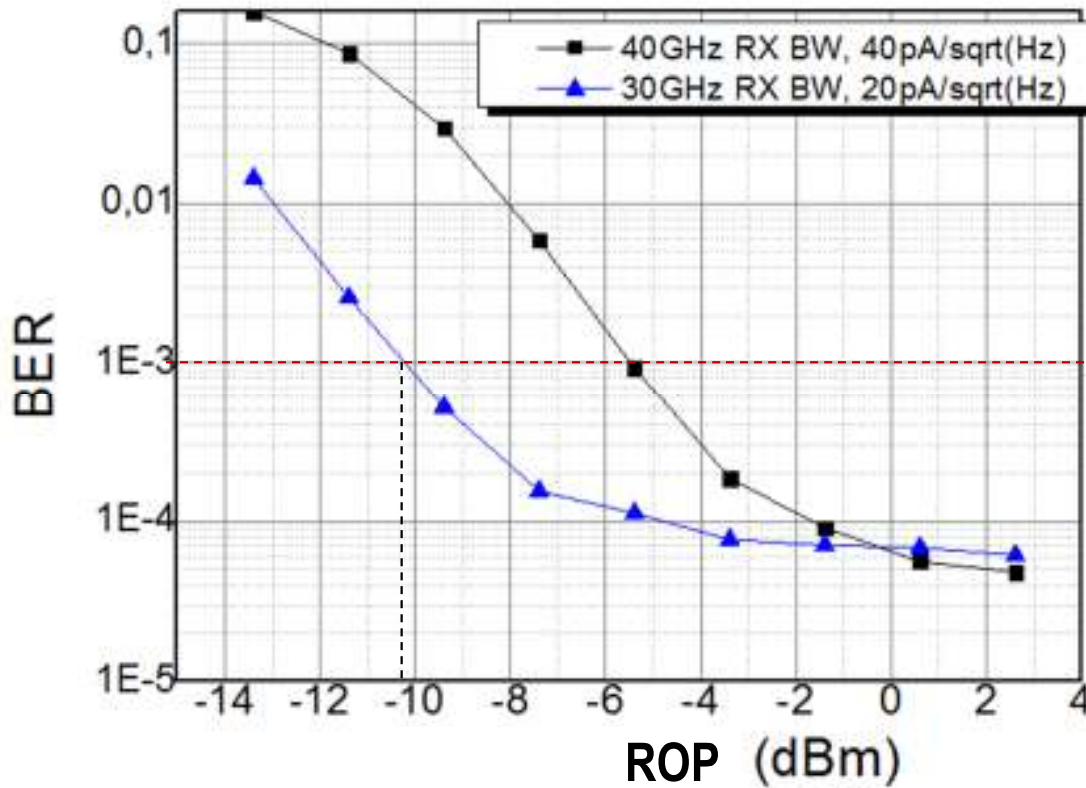
PD+ linear TIA BW= 40GHz

1st-order Bessel approximation of EML, DAC and PD+TIA

5th-order Bessel approximation for ADC, 5 bits ADC ENOB

21-tap T-spaced FFE

Receiver Noise and Bandwidth Effect



(DAC bandwidth= 23GHz)
(ADC bandwidth= 23GHz, ENOB= 5)

Baud rate= 56Gbaud

TX driver AMP BW=31GHz

SNR before EML =21dB

EML BW=32GHz

ER=8dB

WL=1310nm

RIN=-145dB/Hz

10km SSMF

1st-order Bessel approximation of EML,
DAC, PD+TIA, driver amp

PD responsivity =0.8A/W

5th-order Bessel approximation for ADC

21-tap T-spaced FFE

Summary

- **56Gb/s PAM4**

- ADC ENOB and electrical SNR before EML impact error floor

- With DAC BW \geq 14GHz, electrical SNR before EML \geq 21dB, EML BW=31GHz, and ADC BW=25GHz, ENOB=5, an error floor occurs at $<1e-6$

- A pre-FEC threshold of $3e-4$ could close the link budget

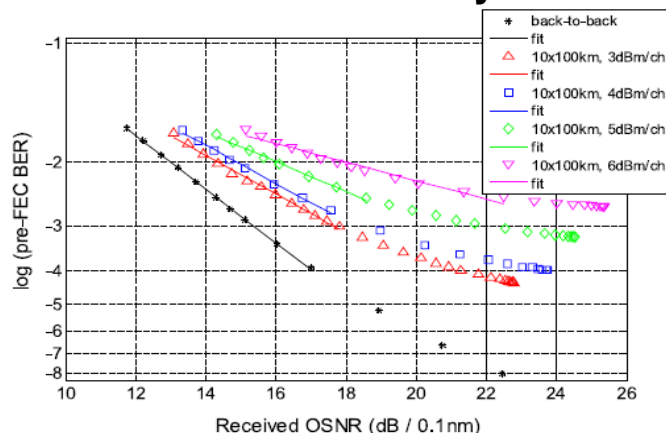
- **112Gb/s PAM4**

- For DAC BW=23GHz, ADC BW=23GHz, ENOB=5, electrical SNR before EML \geq 21dB, EML BW= 32GHz, the error floor occurs at $< 1e-4$

- Receiver responsivity, noise spectral density and bandwidth affect receiver sensitivity significantly

- A pre-FEC threshold of $\geq 1e-3$ would be preferred to close the link budget

- **Error floor is common in today's coherent systems**



(ATT, J. Opt. Commun. Netw, p. B131, Vo.4, Nov 2012)