Test equipment considerations for 400G early implementations

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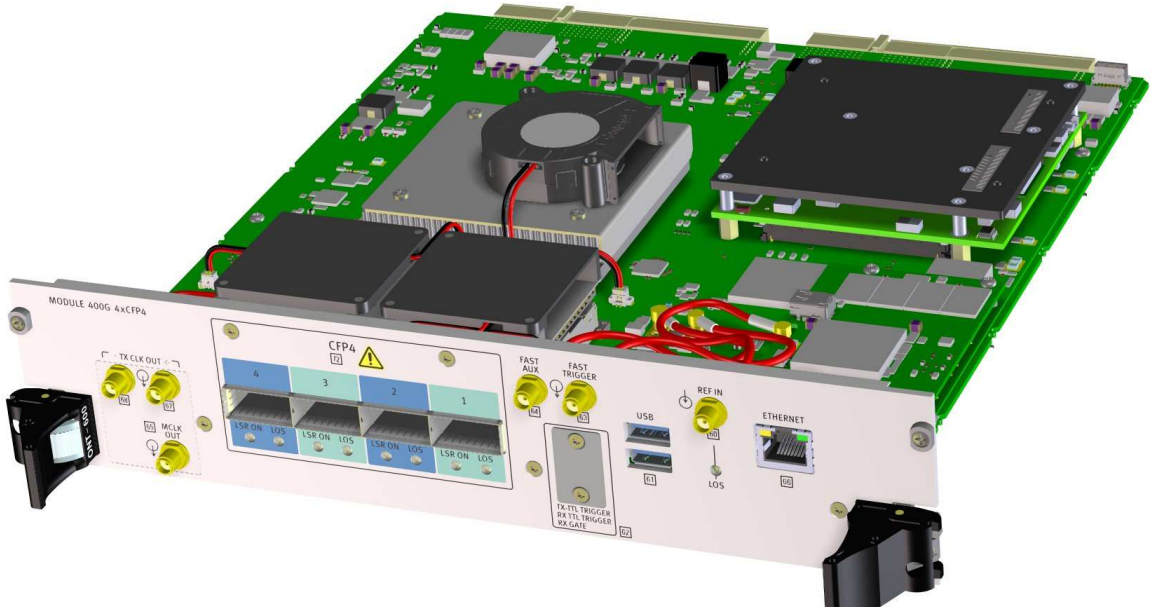
Role of test equipment in standards

- Physical Layer
  - Classic high performance oscilloscopes, VNAs, BERTs
  - Performance influenced by standards
  - Photonic and electrical layer
  - Some very ‘challenging’
    - i.e. SRS – 10G was difficult, 100G no ‘point’ solution (no one box – easy to use & repeatable across ecosystem)
- Protocol + standardized I/F
  - Strongly impacted by standards
  - Covers L2…L7
  - Form factor impact - but can be adapted
    - i.e. CFP => CF2, CFP2 => CFP4 all possible
    - But CFP2 => CFP/CXP not practical

A ‘typical’ protocol aware 400G test set – 1st generation



- Should support appropriate module form factor
  - I/O electrical I/F + MDIO etc
- Protocol aware
  - PCS
  - FEC
  - Ethernet
  - OTN applications

Key applications

- Physical layer
  - Performance, margin and diagnostics
  - Often together with high performance oscilloscope etc
- PCS/FEC
  - Validate PCS layer and alarm + error behavior
- Ethernet/IP
  - Full line rate traffic rate
  - QoS parameters measured and validated
- Advanced transponder test and validation
  - Validate key transponder parameters (many related to IEEE standards)
    - Skew tolerance
  - Seen as critical with more complex transponders (i.e. more than just EO and OE converters)
    - 1st generation CFP & gearbox
    - Edge cases (glitches, service disruption, marginal I/O)

Challenges – FPGA impact

- Protocol aware test equipment is usually based on high end FPGAs
  - Time to market
  - Flexibility
  - Address future protocols and emerging standards
- So products ‘gated’ by FPGA
  - I/O speed (and performance)
  - Size (FEC, PCS, Logic)

- Expectation is to have ‘real’ test equipment ready ~18 months before standard.

Challenges – FPGA I/O

- I/O
  - Current generation FPGA based around 28G NRZ I/O
- PAM-4 etc will need external ‘gearbox’ in the first generation equipment
  - Can limit functionality & delay time to market
  - Skew tolerance (dynamic skew)
  - Jitter (SRS)
- 1st generation 100G used ‘conservative/mature’ 10G I/O and yet industry still had a lot of painful issues
- 25G technology is still emerging 1st/2nd generation parts

Challenges – FPGA impact

- FEC
  - FEC take up a lot of area in an FPGA
    - Langhammer_3bs_01_1114.pdf (order of magnitude greater)
    - And we need area for test functions (typical T&M IP can be x2 great in area than normal functional PCS/MAC
  - => RS is the preferred FEC (over BCH) and must be of reasonable complexity & gain

- PCS/MAC
  - No major concerns – proposals all seem within capabilities of current generation FPGAs

Summary of Key issues

- I/O
  - Anything other than 16 x 25/28G NRZ needs external ‘gearbox’
  - Gates test equipment availability (and performance)
  - Limits test coverage
  - good to have ‘performance gap’
    - i.e. test equipment I/O should be at least x2 better (lower jitter, ISI, skew, symmetry)
- FEC
  - Anything other than RS has a significant impact in FPGA area
- SRS
  - Difficult at 10G NRZ
    - Cohort correlation
    - Calibration & reference receivers
  - No ‘canned’ solution at 25G NRZ
  - Is it really viable as a ‘standard test’ for the future?