# Summary of NRZ CDAUI proposals

Piers Dawe Tom Palkert Jeff Twombly Haoli Qian Mellanox Technologies MoSys Credo Semiconductor Credo Semiconductor

#### Contributors

Scott Irwin Mike Dudek Ali Ghiasi MoSys

QLogic

Ghiasi Quantum LLC

### Introduction

- Builds on "50Gb/s Modulation Proposal", options 1 (and 2)
  - <u>http://ieee802.org/3/bs/public/14\_11/goergen\_3bs\_03a\_1114.pdf</u>
- Addresses project objective
  - "Support optional 400 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications"
- Chip-to-module CDAUI-8
  - Detailed baseline proposal in the style of an annex at <u>http://ieee802.org/3/bs/public/adhoc/elect/14\_1204/palkert\_01a\_1214\_elect.pdf</u>
  - updated to <u>http://ieee802.org/3/bs/public/15\_01/palkert\_3bs\_01\_0115.pdf</u> at this meeting
- Chip-to-chip CDAUI-8
  - Detailed baseline proposal in the style of an annex at <u>http://ieee802.org/3/bs/public/adhoc/elect/14\_1218/palkert\_02\_1214\_elect.pdf</u>
  - updated to <u>http://ieee802.org/3/bs/public/15\_01/palkert\_3bs\_02\_0115.pdf</u> at this meeting
- Both NRZ, both assume 100GBASE-KR4-strength FEC: Clause 91, RS(528,514)

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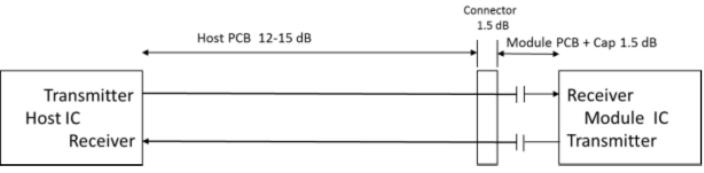
### Motivation

- At each new speed, we introduce something new:
  - 10G lanes: 64B/66B coding, better connectors...
  - 25G lanes: Equalizing reference receiver, better connectors...
- But we end up finding that PAM2 NRZ still works
  - It's well understood
  - It's simple
  - Tolerant to ILD and crosstalk
  - In our estimation, it's lower power than PAM4 for both host and module
    - See <a href="http://ieee802.org/3/bs/public/15\_01/qian\_3bs\_01\_0115.pdf">http://ieee802.org/3/bs/public/15\_01/qian\_3bs\_01\_0115.pdf</a>
    - Lower power because it's simpler
- We expect the same will happen again:
  - 50G lanes: End-to-end FEC , better connectors...
  - Still PAM2 NRZ, as in associated baseline proposals

## Chip-to-module CDAUI-8

- 8 differential lanes, 51.5625 GBd, AC coupled in the module
- Specification and test methodology similar to
  - CEI-56G-VSR
    - oif2014.277.02 in <a href="http://ieee802.org/3/bs/private/oif-cei-56G-1114.zip">http://ieee802.org/3/bs/private/oif-cei-56G-1114.zip</a> ,
  - CEI-28G-VSR
    - <a href="http://www.oiforum.com/public/documents/OIF\_CEI\_03.1.pdf">http://www.oiforum.com/public/documents/OIF\_CEI\_03.1.pdf</a> clause 13,
  - C2M CAUI-4 (802.3bm, Annex 83E),
  - and FC-PI-6
- Compliance points are related to the module connector
  - Compliance boards will have to be specified to higher frequencies
    - And with reduced loss if feasible
- FC-PI-6 experience shows that the channel loss can be increased beyond C2M CAUI-4 when FEC is used
- Proposal includes 1-tap DFE in the reference receiver
  - Trade off between power (DFE or not) and channel loss needs more study

## Chip-to-module CDAUI-8



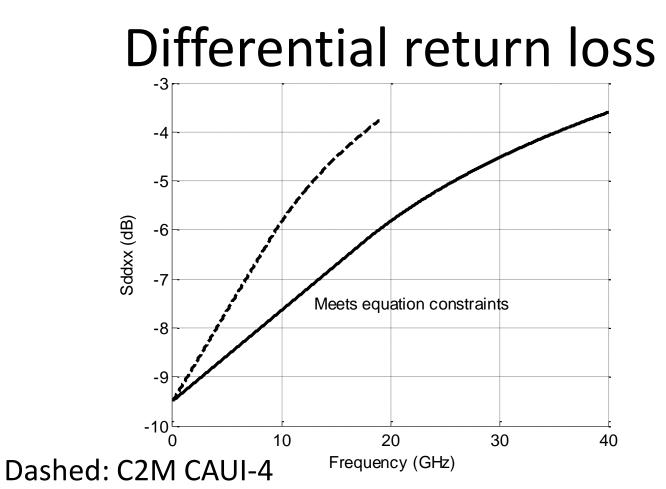
- Max channel loss 15 to 18 (TBD) dB
  - C2M CAUI-4 and CEI-28G-VSR have 10 dB, FC-PI-6 has 15.5 dB
- Max host loss 12 to 15 dB
  - C2M CAUI-4 and CEI-28G-VSR have 7.3 dB, FC-PI-6 has 12.8 dB
- The higher losses are the same channel losses as for C2M CAUI-4, extended to higher frequencies
  - Therefore will support the same distance with the same material
- Or for the same distance, power could be reduced with improved PCB material by removing DFE, using the lower loss limit (~15 dB)
- Spec BER 1e-6 before FEC
  - Very low BER after FEC correction (~1e-25 for random errors)

#### Host and module outputs

- The output eye is measured using a reference receiver with a continuous time linear equalizer (CTLE)...
  - Similar methodology to C2M CAUI-4 etc., but no need to extrapolate the bathtub curves
- And for host output, possibly a DFE in addition
  - For channels above 15 dB?
- CTLE for host output has 12 steps instead of 9
- CTLE for module output has 3 steps instead of 2, no DFE
- Host output eye height 60 mV at 1e-6
  - Compare C2M CAUI-4 with 95, 80 mV at 1e-15
  - Compare FC-PI-6 with 50 mV at 1e-6

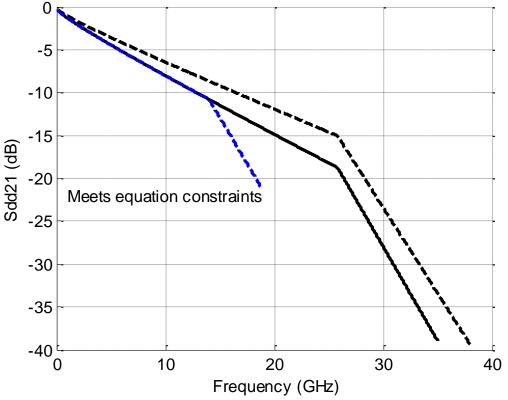
### Host and module inputs

- Module and host input specs follow host and module output specs similarly to C2M CAUI-4
- Host input can be tuned with knowledge of host channel loss or adaptively as host implementer chooses
  - Just like C2M CAUI-4 etc.
- Module input can be tuned adaptively
  - May be able to use a recommended CTLE peaking value (like C2M CAUI-4) as a starting point and/or sanity check
  - NRZ likely to be more tolerant to mis-tuning than PAM4



- Solid: Candidate for C2M CDAUI-8 (C2M CAUI-4 scaled for signalling rate)
  - Will need adjustment when feasible connector, package and compliance board improvements can be quantified

#### Channel differential insertion loss



- Blue: C2M CAUI-4
- Solid: Candidate for C2M CDAUI-8 (reference receiver with DFE)
- Dashed: lower power non-DFE candidate for C2M CDAUI-8

## Chip-to-chip CDAUI-8

- 8 differential lanes, 51.5625 GBd, AC coupled
- Specification and test methodology similar to C2C CAUI-4 (802.3bm, Annex 83D)
- These are the same channel loss as for C2C CAUI-4, extended to higher frequencies
  - Therefore will support the same distance ("25 cm")
  - Up to one connector
- Compliance points are related to the ICs
- Same 3-tap Tx emphasis setting method as C2C CAUI-4
  - Stronger post-cursor than C2C CAUI-4, similar to 100GBASE-KR4
- Spec BER 1e-6 before FEC
  - Very low BER after FEC correction
- Channel is defined by COM
  - COM reference receiver has up to 12 dB continuous time filter (like C2C CAUI-4 and 100GBASE-KR4) and 5-tap DFE (like C2C CAUI-4)

## Chip-to-chip CDAUI-8

- Receiver interference tolerance test insertion loss 31 to 32 dB
  - Compare C2C CAUI-4 with 19.5 to 20.5 dB (without FEC, 5 DFE taps)
  - Compare 100GBASE-KR4 with 35 dB (with FEC, 14 DFE taps)
- COM parameters follow Tx specs
  - Allow stronger Tx emphasis than C2C CAUI-4
  - CTLE is scaled for signalling rate
- Return loss specs are TBD
- Summary: very like C2C CAUI-4, use of FEC and stronger Tx emphasis allows more dB of loss

#### Conclusion

- FEC and stronger equalization allows the methodologies of C2M and C2C CAUI-4 to be extended to double the signalling rate
- Preserves the electrical channel lengths of CAUI-4 and the well-known advantages of NRZ signalling