# Updated Models – FEC Cores

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# Overview

- Motivation
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- FPGA ⇔ ASIC Scaling - Updated
- FPGA and ASIC Latency - Implications
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# Motivation

- Modelling and scaling methodology introduced in langhammer_3bs_01_1114 taken as baseline by multiple FEC users
- Stronger FECs being considered can be very large compared to 802.3bj FECs
- Current model may be pessimistic for stronger FECs
  - May indicate prohibitive cost for FPGA
- Previous FPGA to ASIC conversion factor too coarse
- Divergence in FPGA and ASIC implementation
  - Impact of block marking on relative latency
- Multi-lane aggregation may be sub-linear
  - FPGA and ASIC methods differ

# Area Scaling - Updated

- Modelled relative FPGA areas
  - KR4: 1.0
  - KP4: 2.9
  - RS(560,514): 6
  - RS(576,514): 10
- Actual relative FPGA areas
  - KP4: 2.5
  - RS(560,514): 4.8
  - RS(576,514): 7.5
- Why?
  - Largest component variance in KES
    - Some subcomponents scale with $t$, not $t^2$
  - Use a KES scaling factor of 0.7
  - New equation: $(0.2*(t_1/t_2)) + (0.28*(t_1/t_2)^2) + (0.3*(t_1/t_2))$

***FPGA/ASIC scaling for stronger FECs? No – largely due to latency mitigation.***

- Actual relative ASIC areas[1]
  - KP4: 2.9
  - RS(560,514): 14.5
  - RS(576,514): 33.4

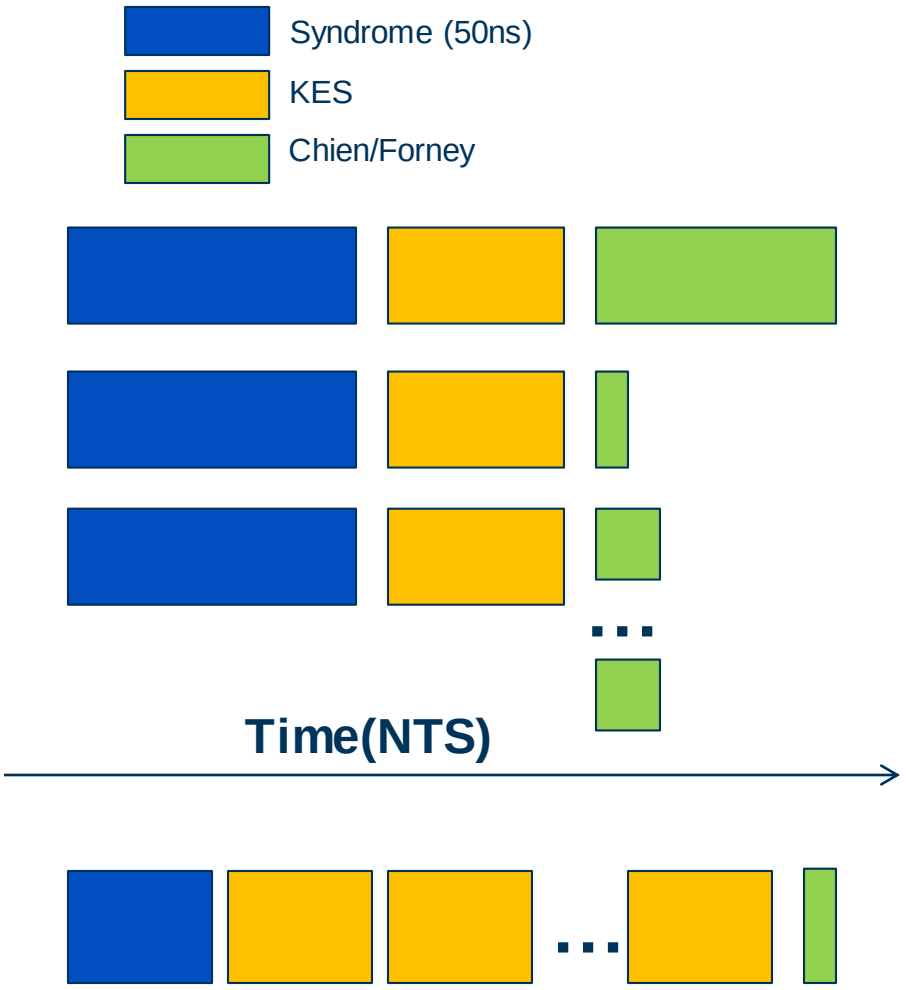
*1. wang_x_3bs_01_0115*

# FPGA ⇔ ASIC Scaling - Updated

- Earlier model too coarse – 10K 6LUTs ⇔ 250KG – 25 gates/6LUT
  - Did not consider all architectural and latency differences
    - ASIC design will be more complex (see latency implications)
  - Did not consider frequency differences
    - FPGA ½ frequency of ASIC
    - But only absolute area matters
- Compare against reported values in gustlin_3bs_03_0115
  - Average absolute difference about 12 gates/6LUT
    - Compared only by reported values
  - Modelled FPGA vs. reported ASIC BCH (2288,2048) agrees
    - 90K 6LUT ⇔ 980 KG

# FPGA and ASIC Latency - Implications

- ASIC KES 2t cycles for smaller codes
- 2t @ 644MHz < 50ns
- Block marking 50ns
  - No block marking << 50ns
- If low latency block marking needed, can parallelize Chien
  - Model assumes 40% of core is Chien/Forney
- If parallelized 4x, FEC Core >2x area




- FPGA KES 8t cycles for smaller codes
- 8t @ 325MHz >> 50ns
- Block marking 50ns
  - Non-material latency increase
- Block marking parallelism will have non-material latency decrease

# FEC Core Aggregation

- 400G FEC first order size is 4x100G FEC
  - This is a single core that supports 4x100G, not 1x400G
- Several ways of aggregating FECs to save area
- Deeper FPGA KES pipeline will allow processing interleaving
- 20%-40% area reduction possible
- Not available in ASIC
  - aggregation example in gustlin_3bs_03_1115 is 1x400G, not 400G = 4x100G
- Current KR4 400G = 4x10.6K 6LUT = 42K 6LUT
  - Possible 25K-30K 6 LUT target
- Current RS(576,514) 400G = 4x75K 6LUT = 300K 6LUT
  - Possible 180K-240K 6LUT target
    - Material consideration for FPGA implementation

# Conclusions

- FPGA stronger FECs expensive, but better than original model estimates
- Block marking and latency optimization can affect area significantly
  - ASIC consideration
  - Longer FPGA latencies will gain little benefit from block marking
- 4x100G FEC in FPGA will benefit from aggregation scaling

# Thank You