Proposed Baseline text for: Chip-to-module 400 Gb/s eight-lane Attachment Unit Interface (CDAUI-8)

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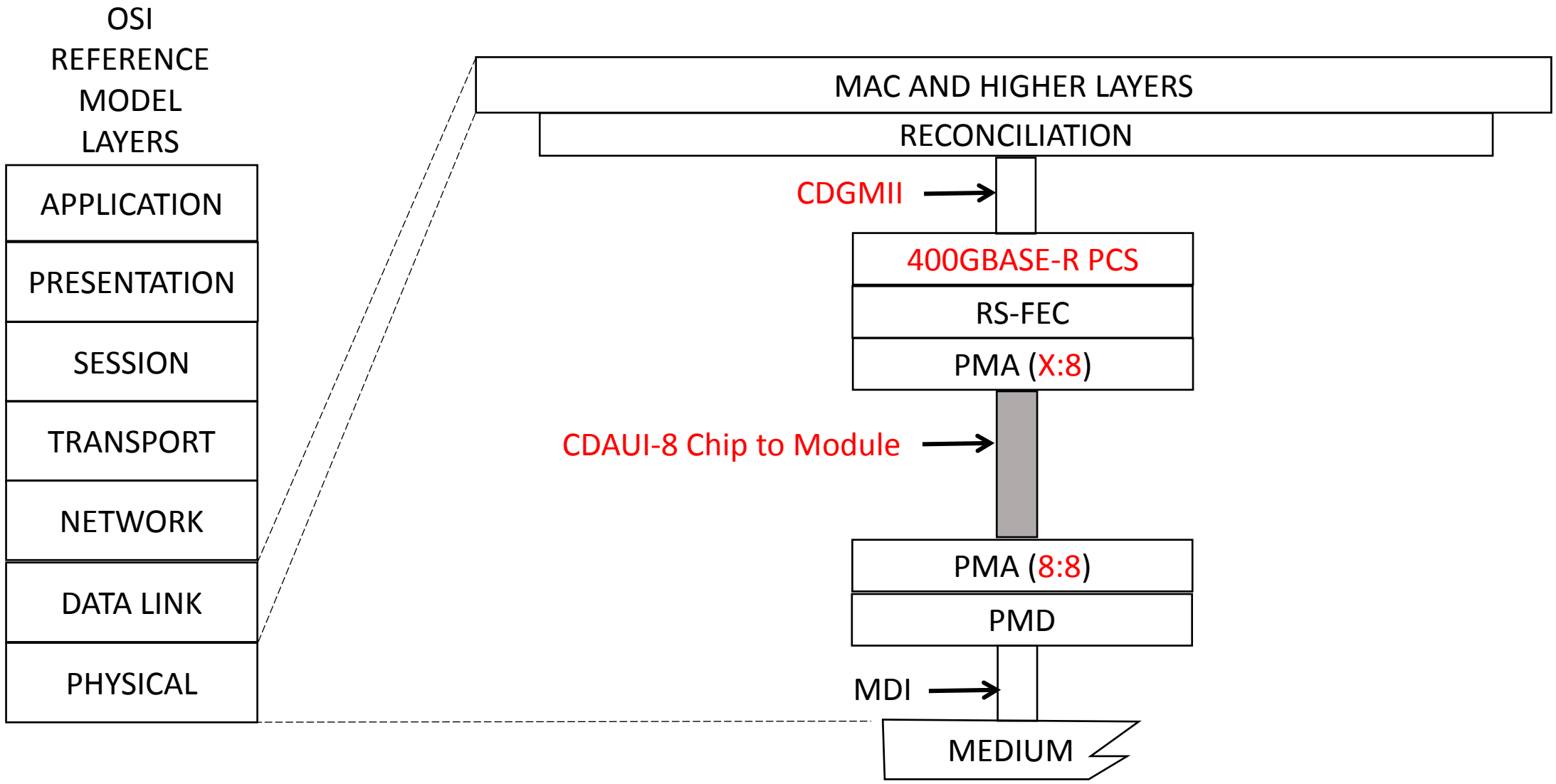
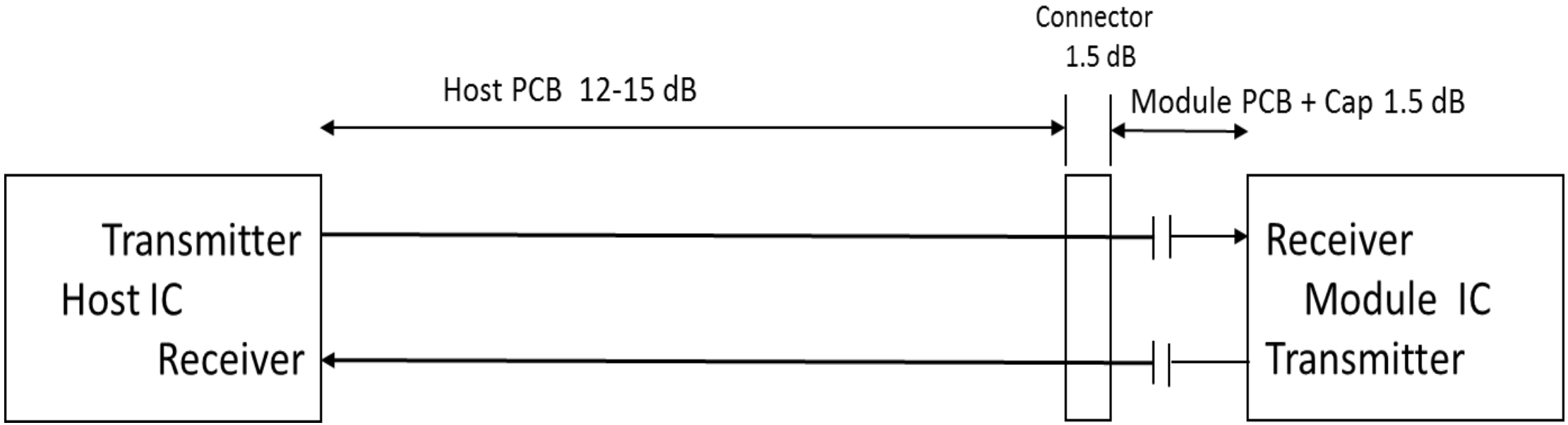
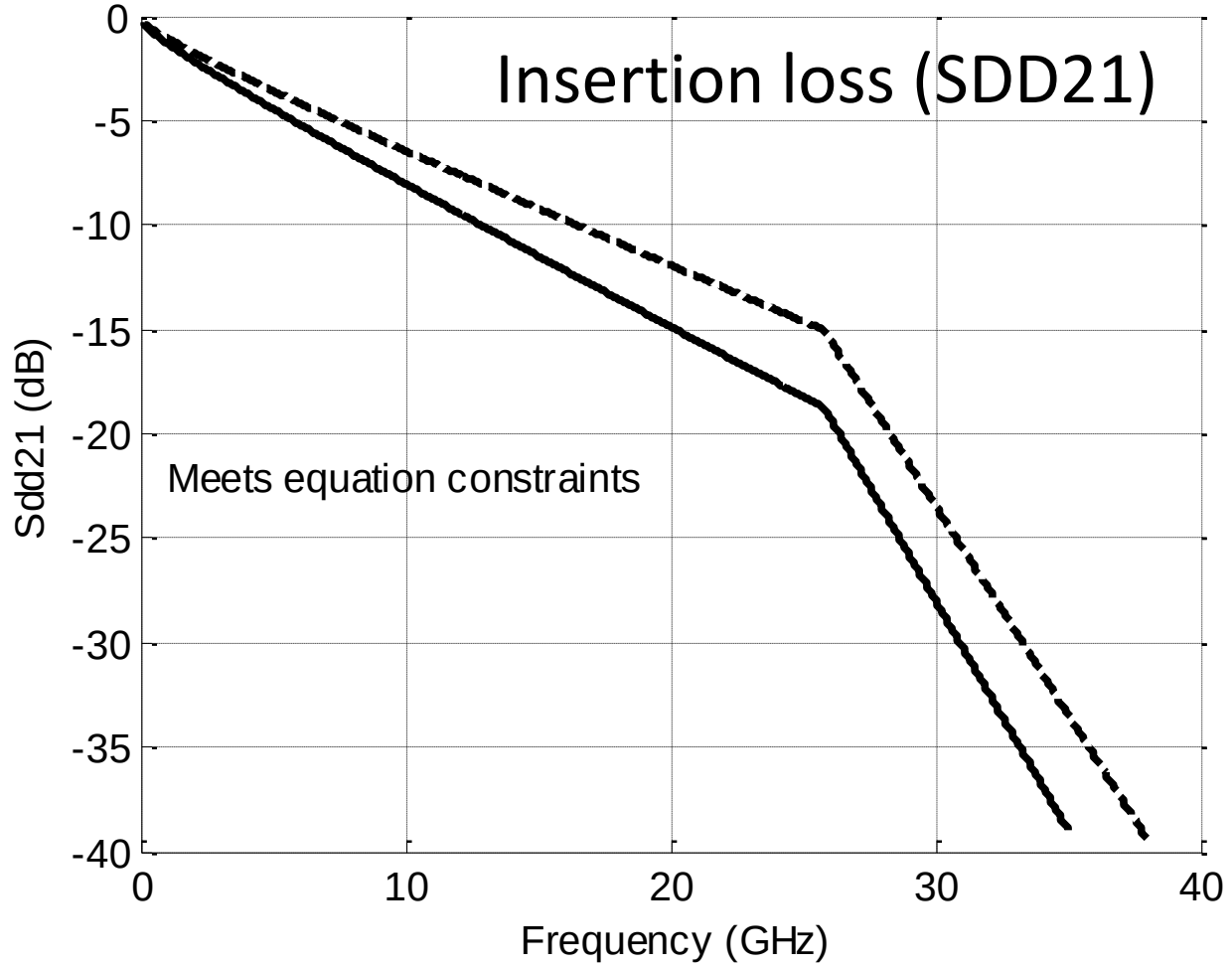


Figure B–1—Example CDAUI-8 chip-to-module relationship to the ISO/IEC Open System Interconnection reference model and the IEEE 802.3 CSMA/CD LAN model

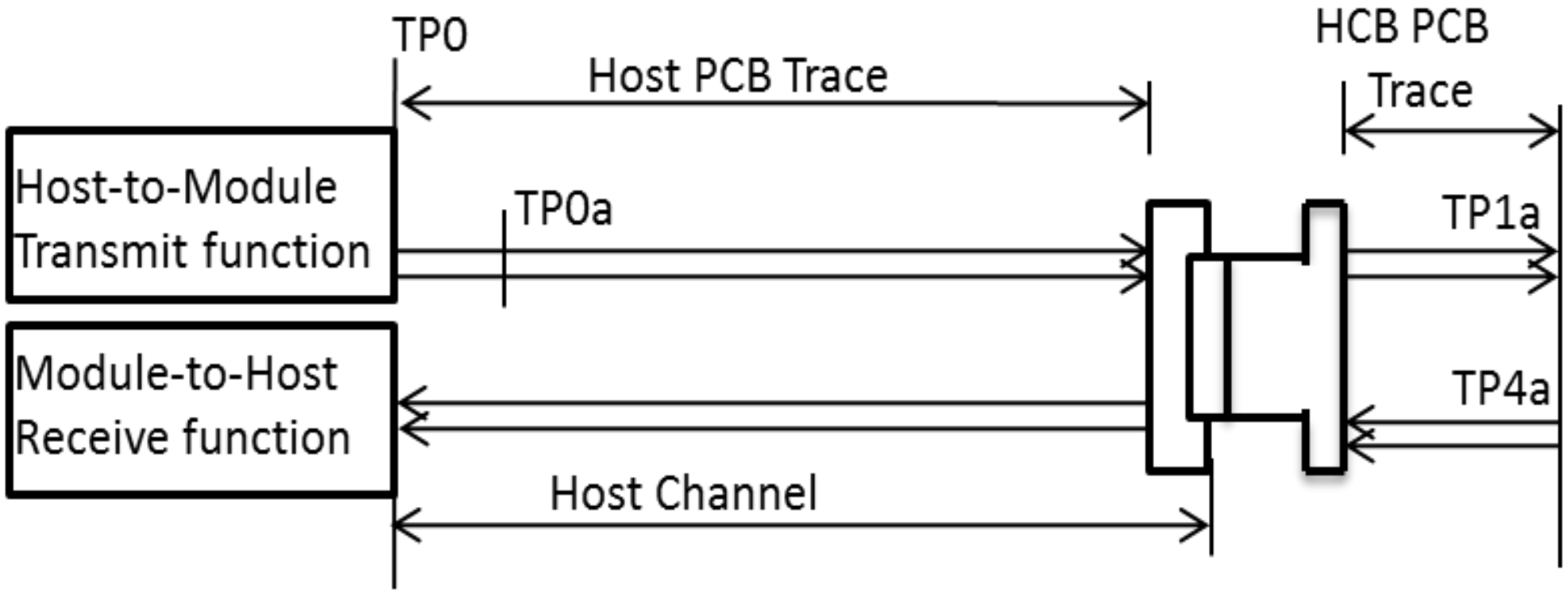


Chip to Module insertion loss budget at 25 GHz

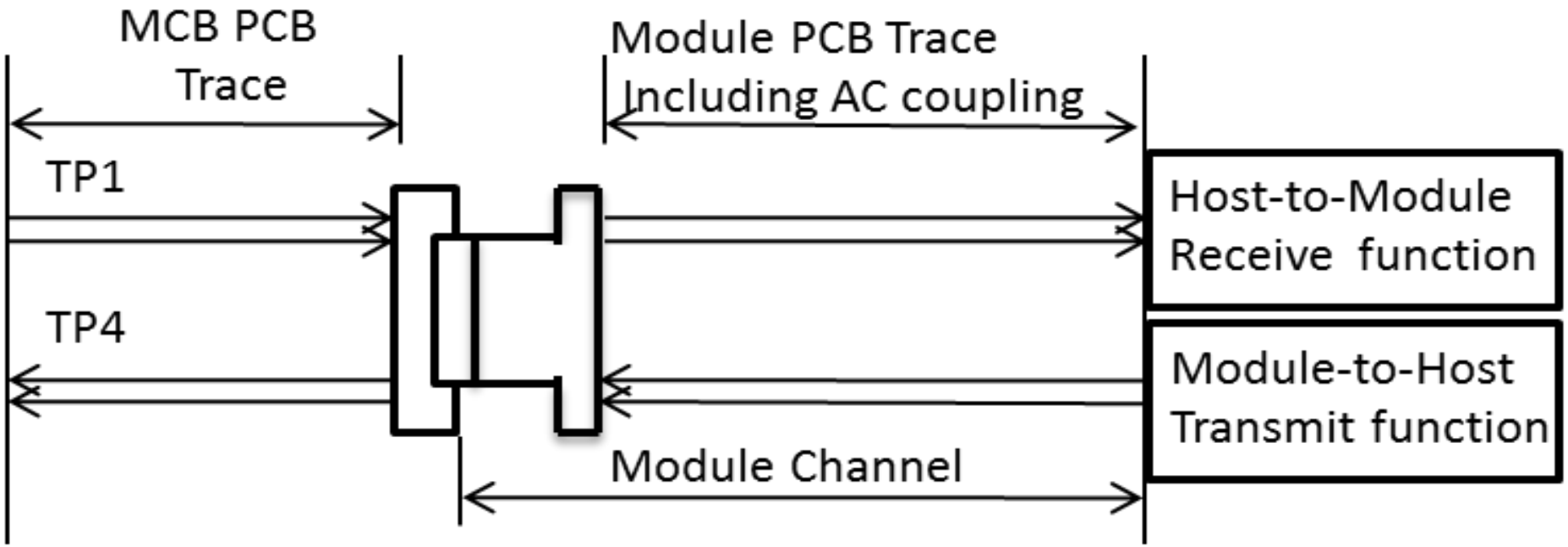


- Solid: $1.076*(0.075 + 0.537\sqrt{f} + 0.566f)$ 10 MHz to 25.78 GHz
- $-38 + 2.2f$ 25.78 GHz to 35 GHz

- Dashed: $0.0807 + 0.4626\sqrt{f} + 0.4876f$ 10 MHz to 25.78 GHz
- $-36.56 + 2f$ 25.78 GHz to 38 GHz



Host CDAUI-8 Compliance points

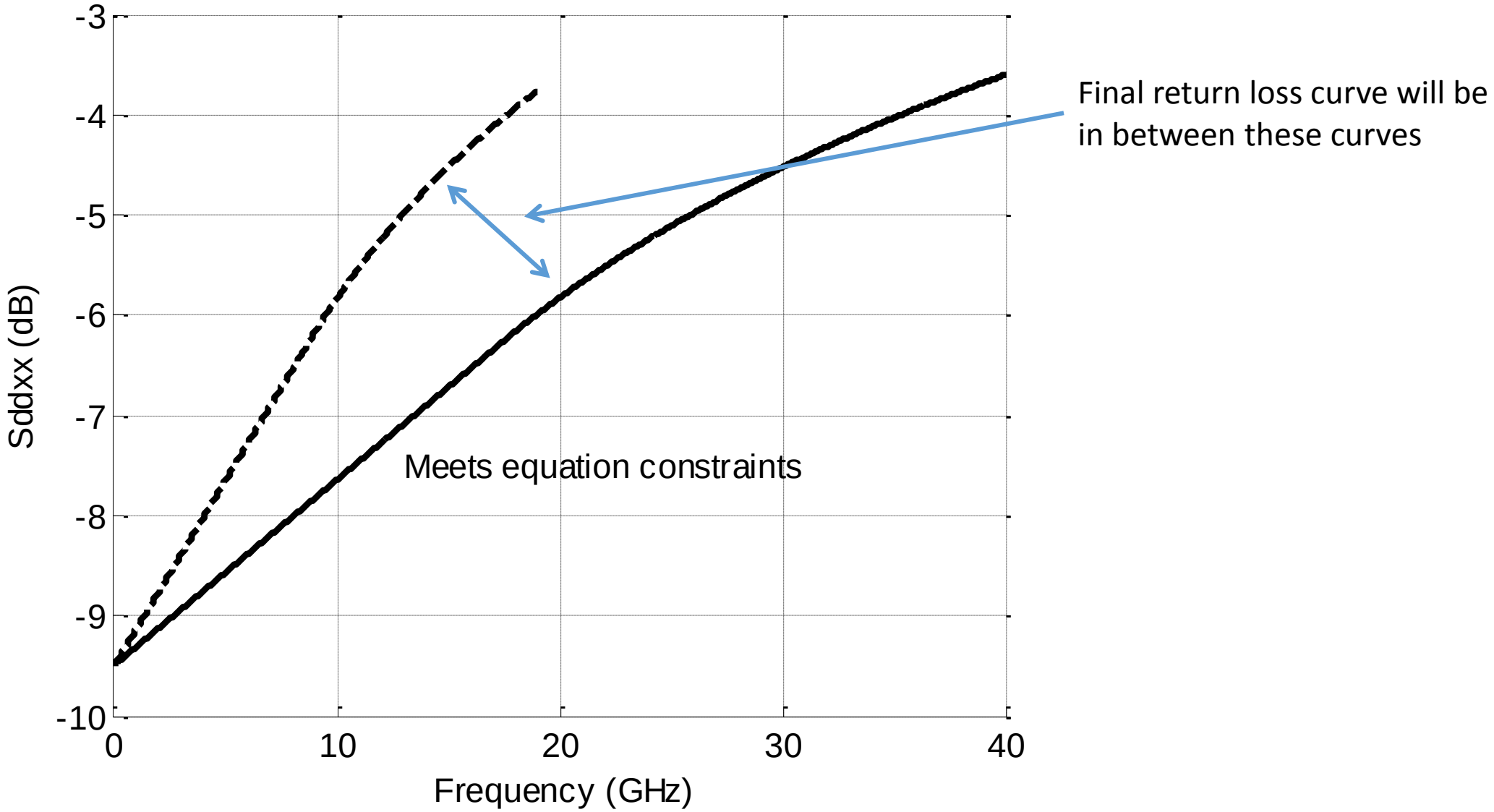


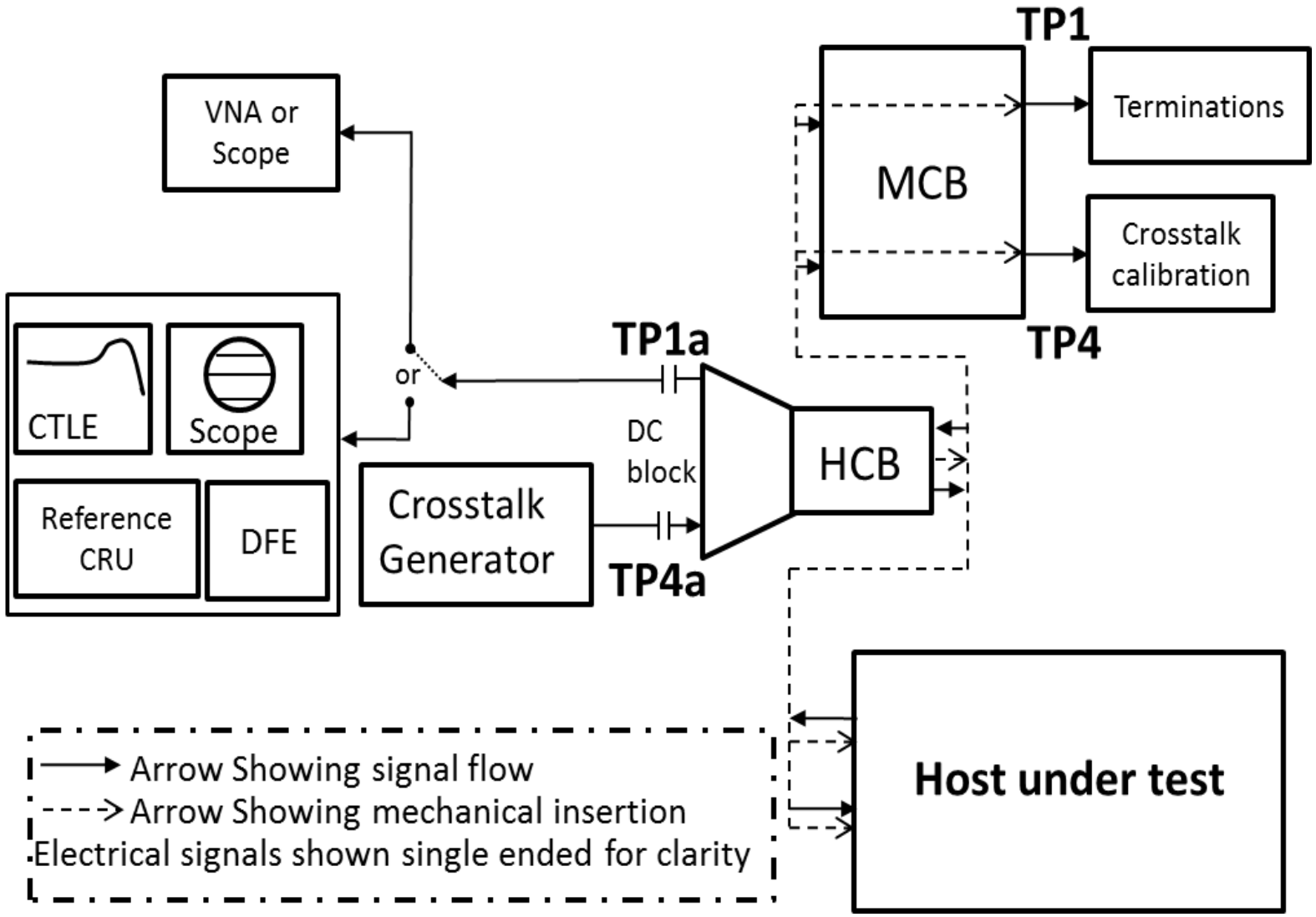
Module CDAUI-8 compliance points

CDAUI-8 host output characteristics (at TP1a)

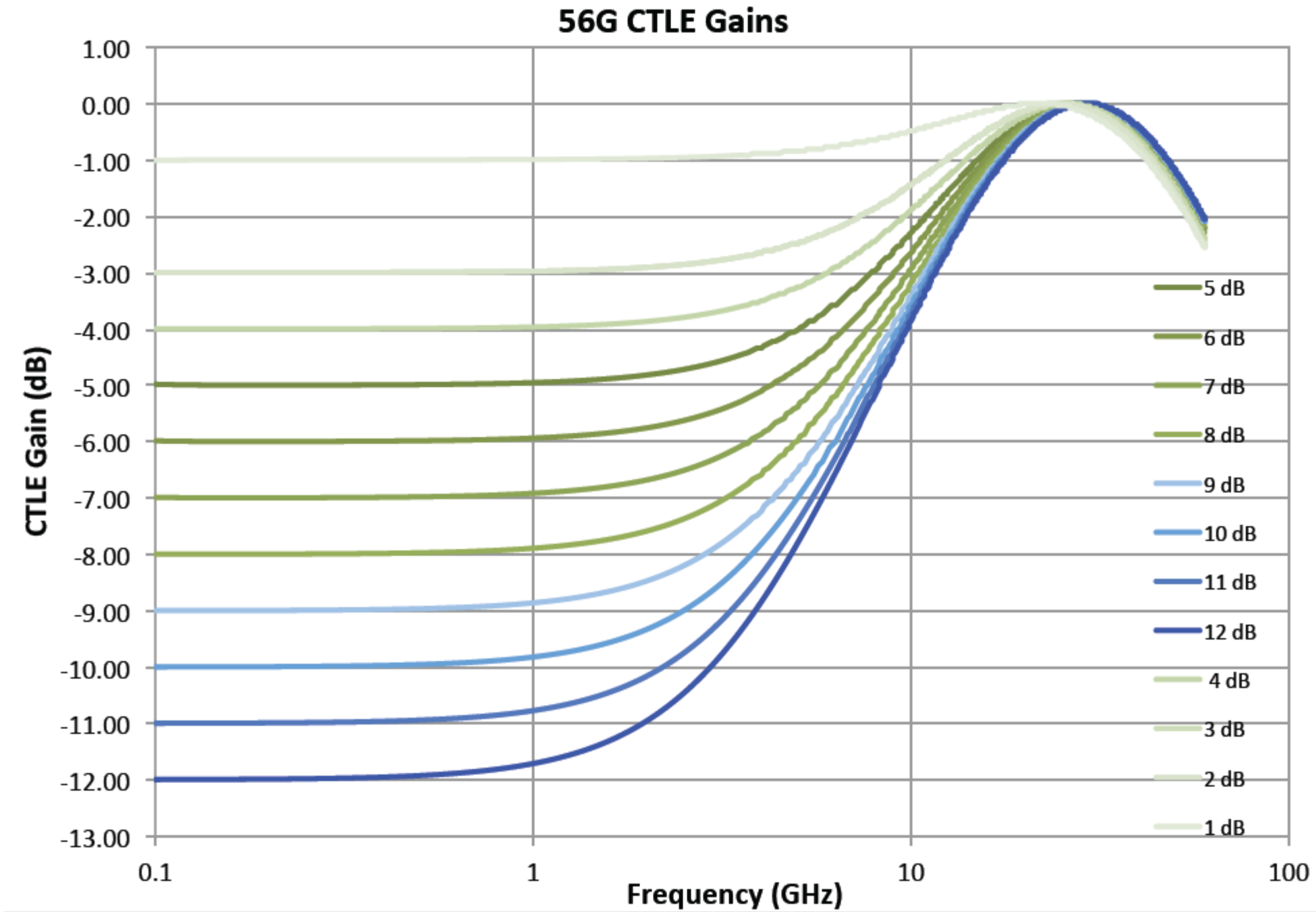
Parameter	Reference	Value	Units
Signaling rate per lane (range)	3.1.1	51.5625 ±100ppm	GBd
DC common-mode output voltage (max)	3.1.2	2.8	V
DC common-mode output voltage (min)	3.1.2	-0.3	V
Single-ended output voltage (max)	3.1.2	3.3	V
Single-ended output voltage (min)	3.1.2	-0.4	V
AC common-mode output voltage (max, RMS)	3.1.2	17.5	mV
Differential peak-to-peak output voltage (max)	3.1.2		mV
Transmitter disabled		35	
Transmitter enabled		900	
Eye width (min)	3.1.6	0.46	UI
Eye height A, differential (min)	3.1.6	60	mV
Eye height B, differential (min)	3.1.6	60	mV
Differential output return loss (min)	3.1.3	Equation 2	dB
Common to differential mode conversion return loss (min)	3.1.3	Equation 3	dB
Differential termination mismatch (max)	3.1.4	10	%
Transition time (min, 20% to 80%)	3.1.5	9	ps

Differential input return loss





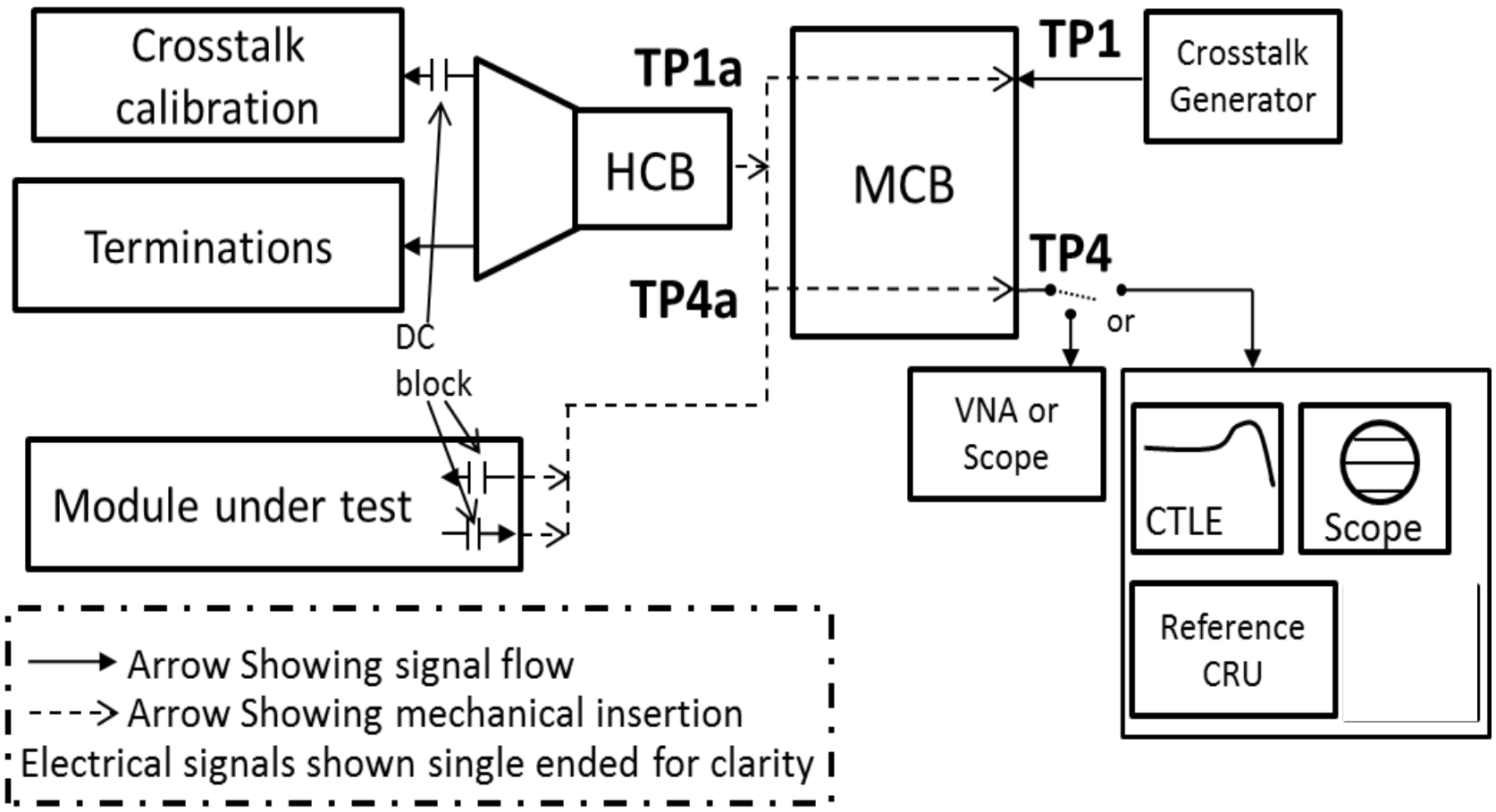
Example host output test configuration


56G CTLE Gains
1.00
0.00
-1.00
-2.00
-3.00
-4.00
-5.00
-6.00
-7.00
-8.00
-9.00
-10.00
-11.00
-12.00
-13.00
CTLE Gain (dB)
0.1
1
10
100
Frequency (GHz)
5 dB
6 dB
7 dB
8 dB
9 dB
10 dB
11 dB
12 dB
4 dB
3 dB
2 dB
1 dB

CDAUI-8 module output characteristics (at TP4)

Parameter	Reference	Value	Units
Signaling rate per lane (range)	3.1.1	51.5625 ±100ppm	GBd
AC common-mode output voltage (max, RMS)	3.1.2	17.5	mV
Differential output voltage (max)	3.1.2	900	mV
Eye width (min)	3.2.1	.57	UI
Eye height, differential (min)	3.2.1	228	mV
Vertical eye closure (max)	4.2.1	5.5	dB
Differential output return loss (min)	3.1.3	Equation 2	dB
Common to differential mode conversion return loss (min)	3.1.3	Equation 3	dB
Differential termination mismatch (max)	3.1.4	10	%
Transition time (min, 20% to 80%)	3.1.5	9	ps
DC common mode voltage (min)[a]	3.1.2	-350	mV
DC common mode voltage (max)[a]	3.1.2	2850	mV

[a]DC common mode voltage is generated by the host. Specification includes effects of ground offset



Example module output test configuration

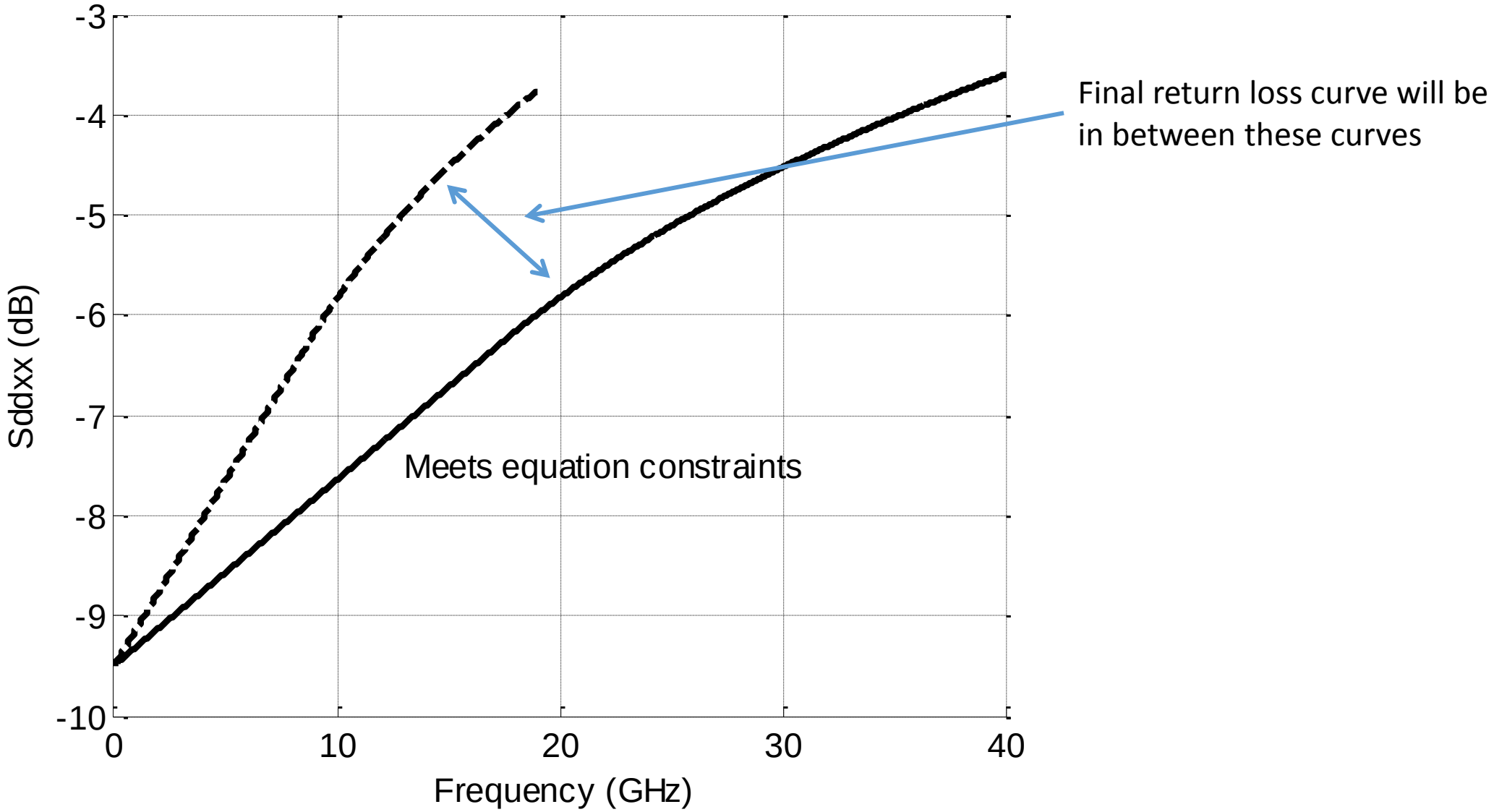
CDAUI-8 host input characteristics

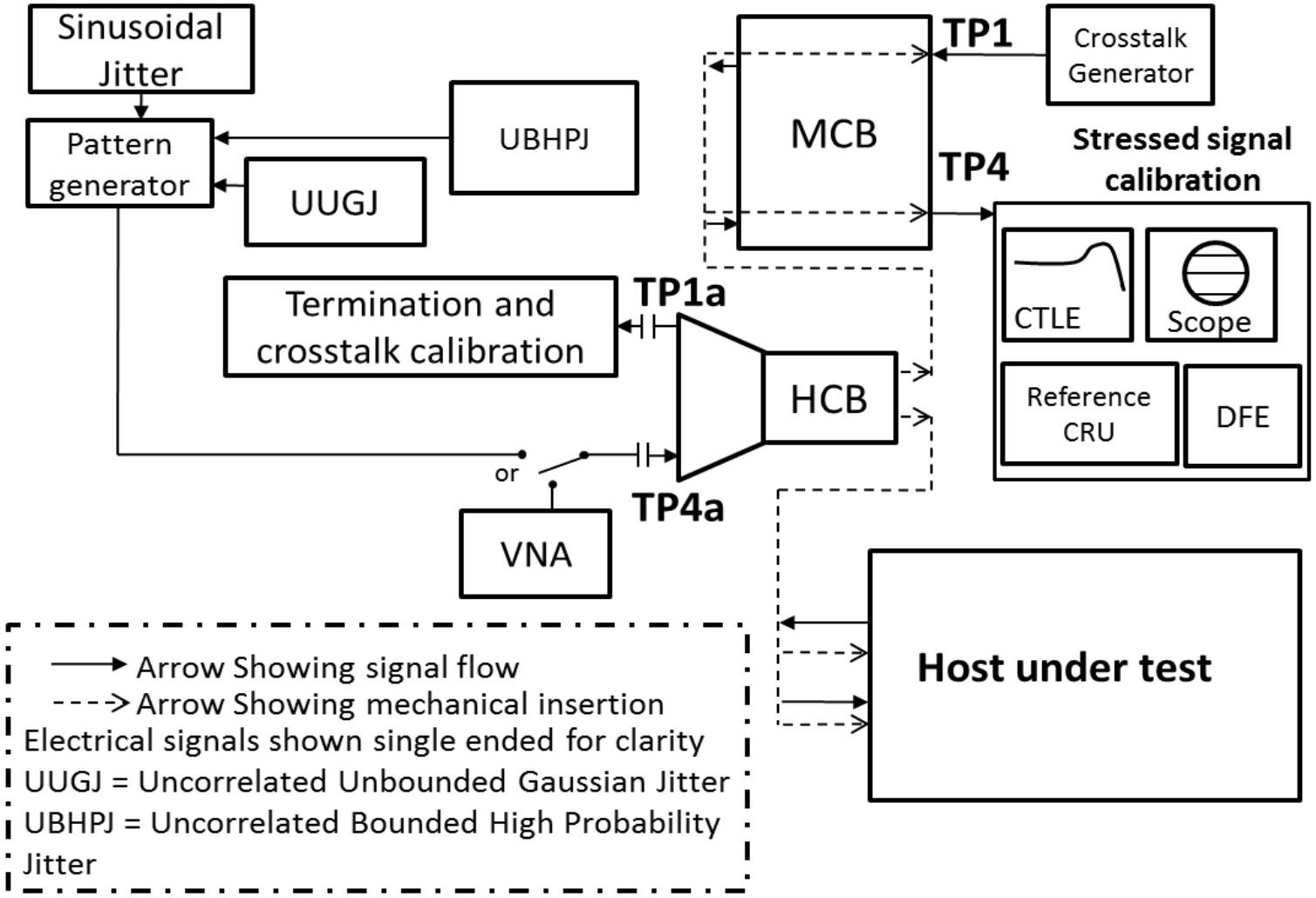
Parameter	Reference	Test point	Value	Units
Signaling rate, per lane (range)	3.1.1	TP4a	51.5625 ±100	GBd
Differential pk-pk input voltage tolerance (min)	3.1.2	TP4	900	mV
Differential input return loss (min)	3.3.1	TP4a	Equation 5	dB
Differential to common mode input return loss (min)	3.3.1	TP4a	Equation 6	dB
Host stressed input testa	3.3.2	TP4	See 99E.3.3.2	
Differential termination mismatch (max)	3.1.4	TP4a	10	%
Common-mode voltage[b] **Min** **Max**	3.1.2	TP4a	 -0.3 2.8	V

[a]Meets BER specified in E.1.1

[b]Generated by host, referred to host ground

Differential input return loss





Example host stressed input test

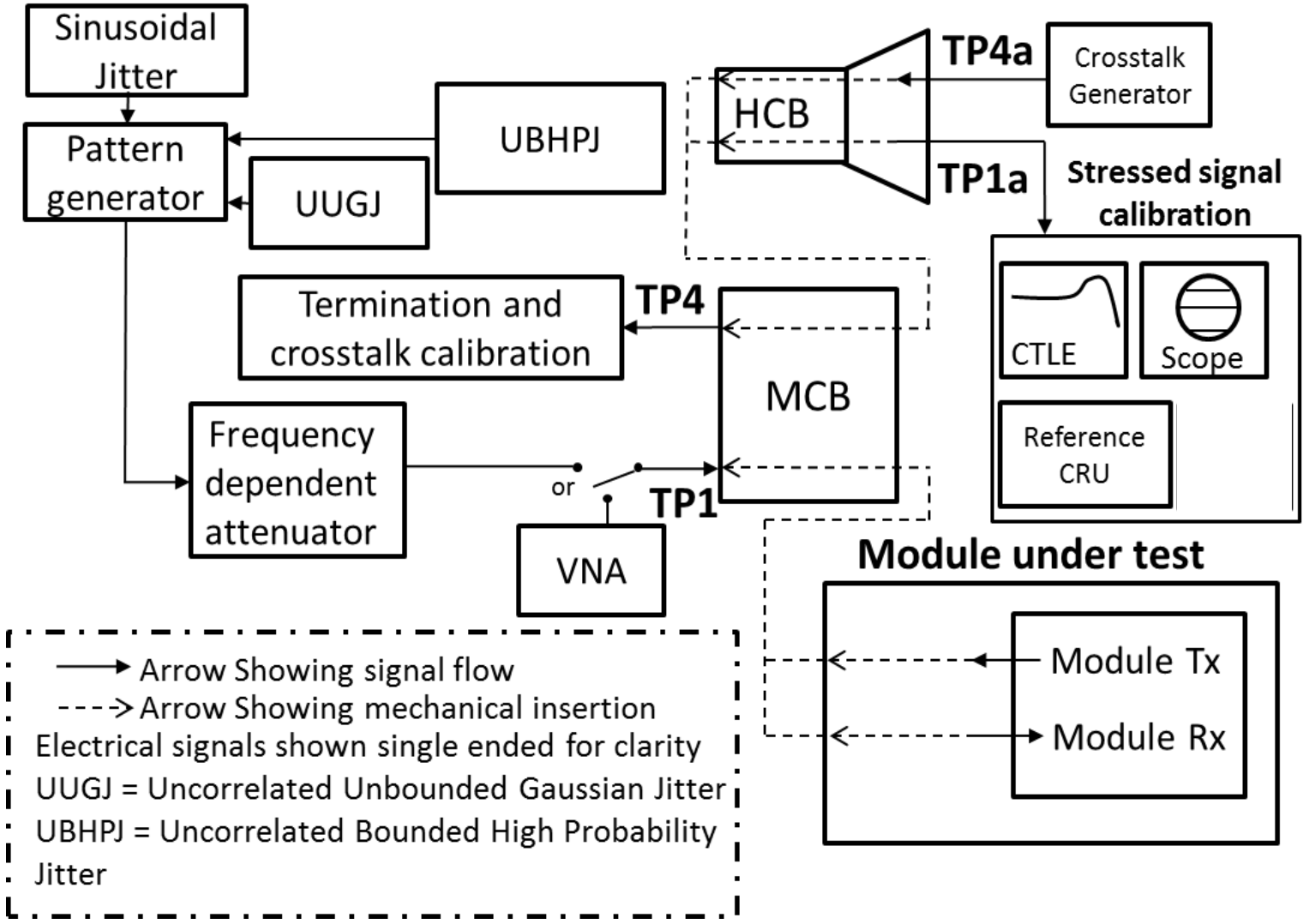
Parameter	Value
Eye width	0.57 UI
Applied pk-pk sinusoidal jitter	Table 88-13
Eye Height	228 mV

CDAUI-8 Module input Characteristics

Parameter	Reference	Test point	Value	Units
Signaling rate per lane (range)	3.1.1	TP1	51.5625 ±100	GBd
Differential pk-pk input voltage tolerance (min)	3.1.2	TP1a	900	mV
Differential input return loss (min)	3.3.1	TP1	Equation 5	dB
Differential to common mode input return loss (min)	3.3.1	TP1	Equation 6	dB
Differential termination mismatch (max)	3.1.4	TP1	10	%
Module stressed input test[a]	3.4.1	TP1a	See 3.4.1	
Single-ended voltage tolerance range (min)	3.1.2	TP1a	-0.4 to 3.3	V
DC common mode voltage (min)[b]	3.1.2	TP1	-350	mV
DC common mode voltage (max)[b]	3.1.2	TP1	2850	mV

[a]Meets BER specified in 1.1

[b]DC common mode voltage generated by host. Specification includes effects of ground offset voltage.



Example module stressed input test

Parameter	Value
Eye width	0.46 UI
Applied pk-pk sinusoidal jitter	Table 88-13
Eye Height	60 mV