Proposed Baseline text for: Chip-to-chip 400 Gb/s eight-lane Attachment Unit Interface (CDAUI-8)

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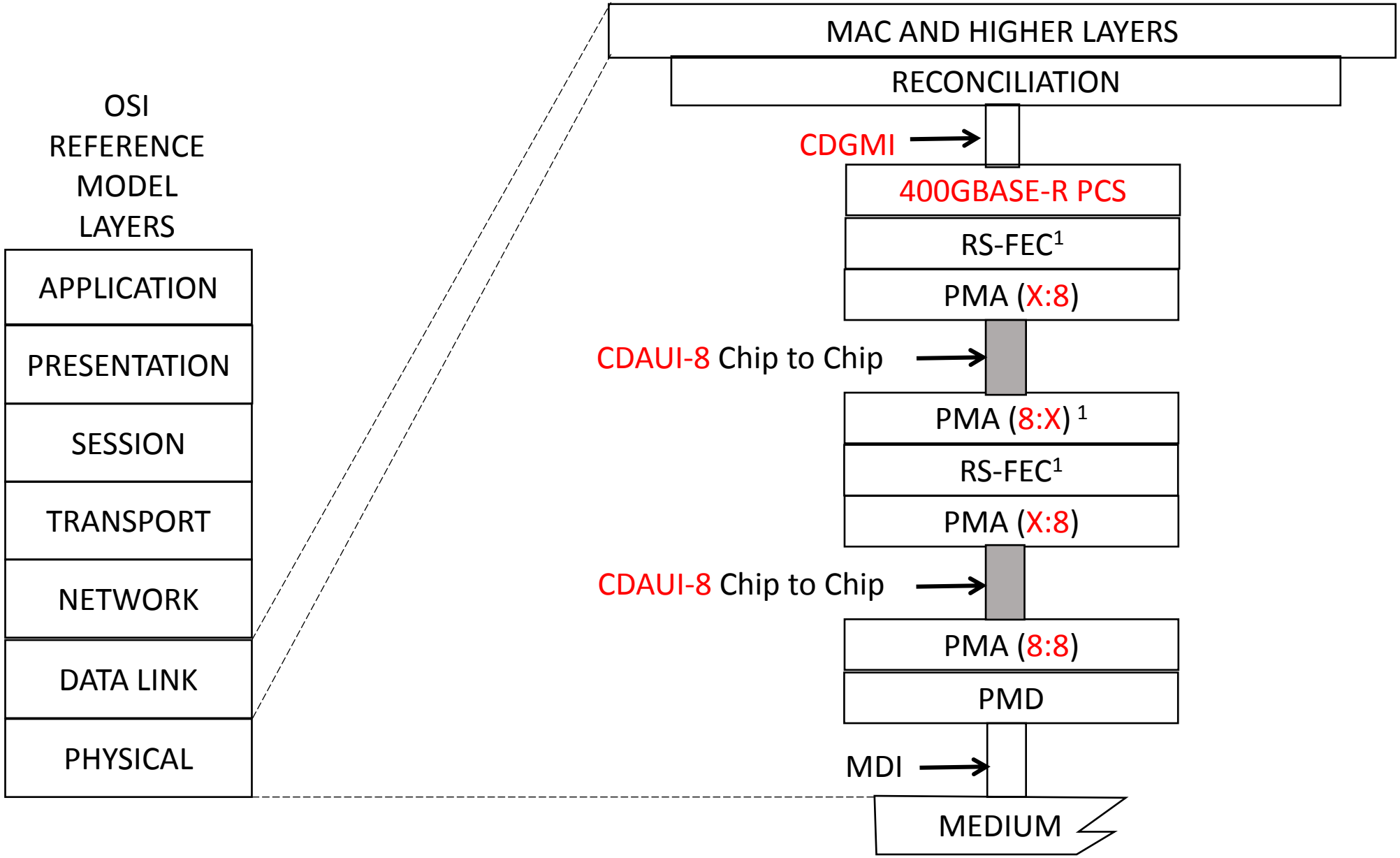
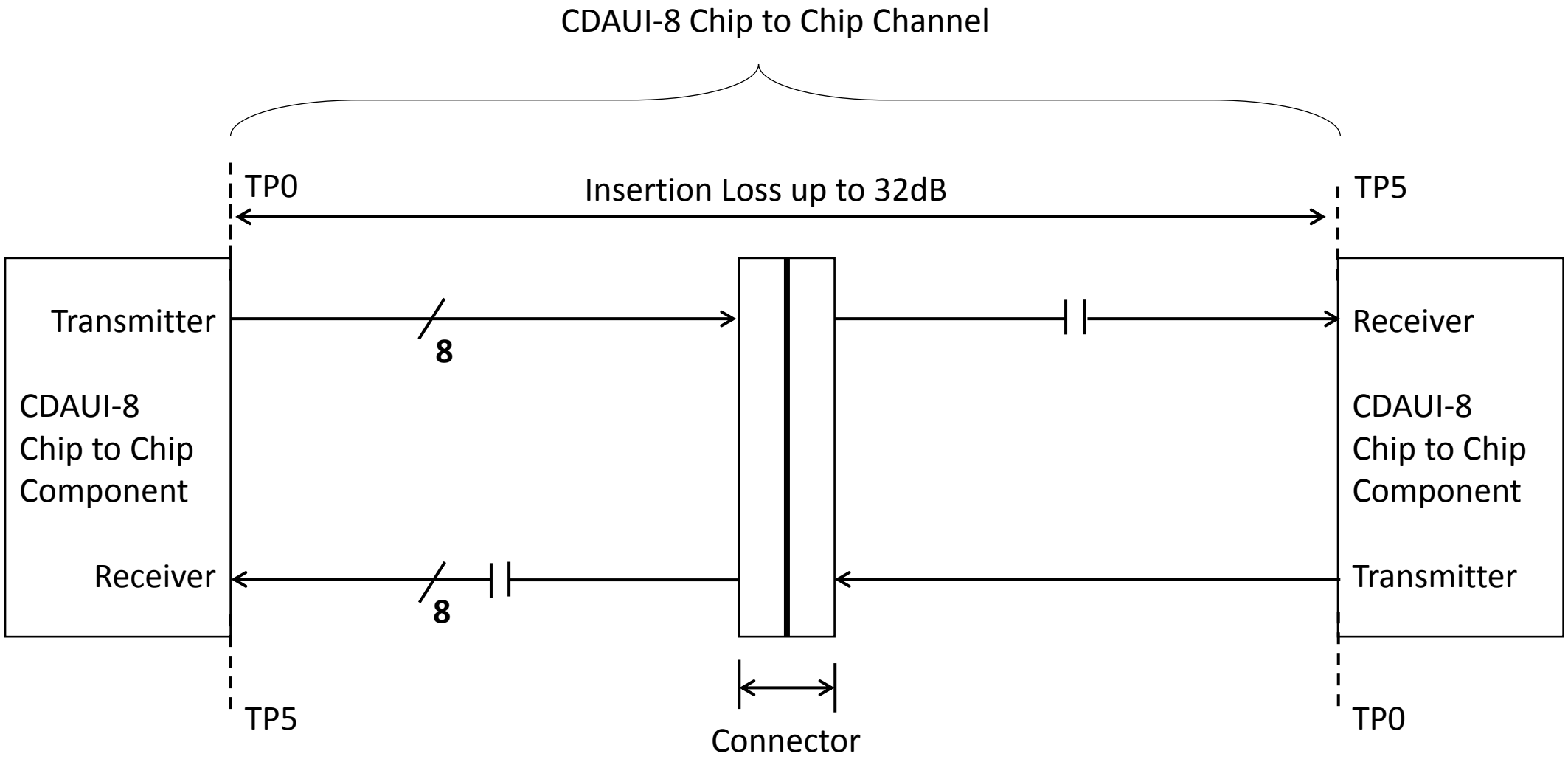
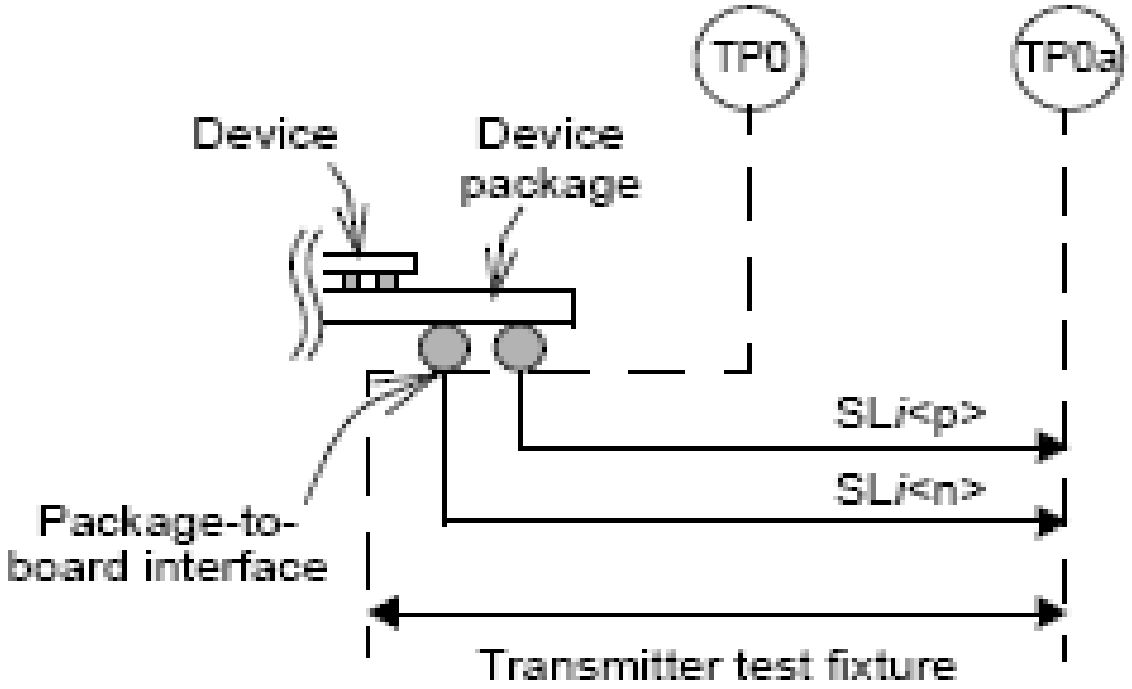


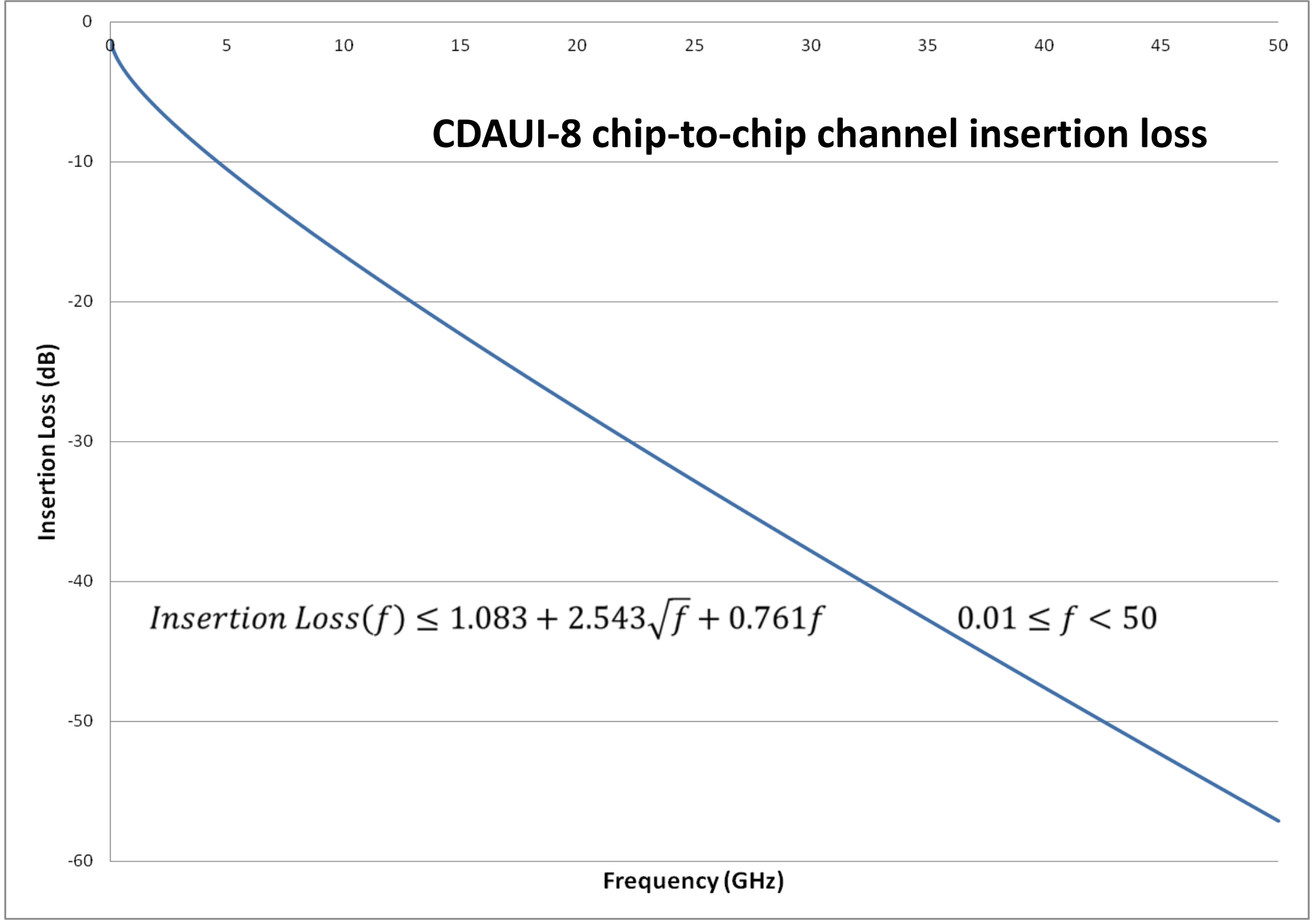
Figure C–1—Example CDAUI-8 chip-to-chip relationship to the ISO/IEC Open System Interconnection reference model and the IEEE 802.3 CSMA/CD LAN model



Chip to chip insertion loss budget at 25 GHz



CDAUI-8 Transmitter Compliance points

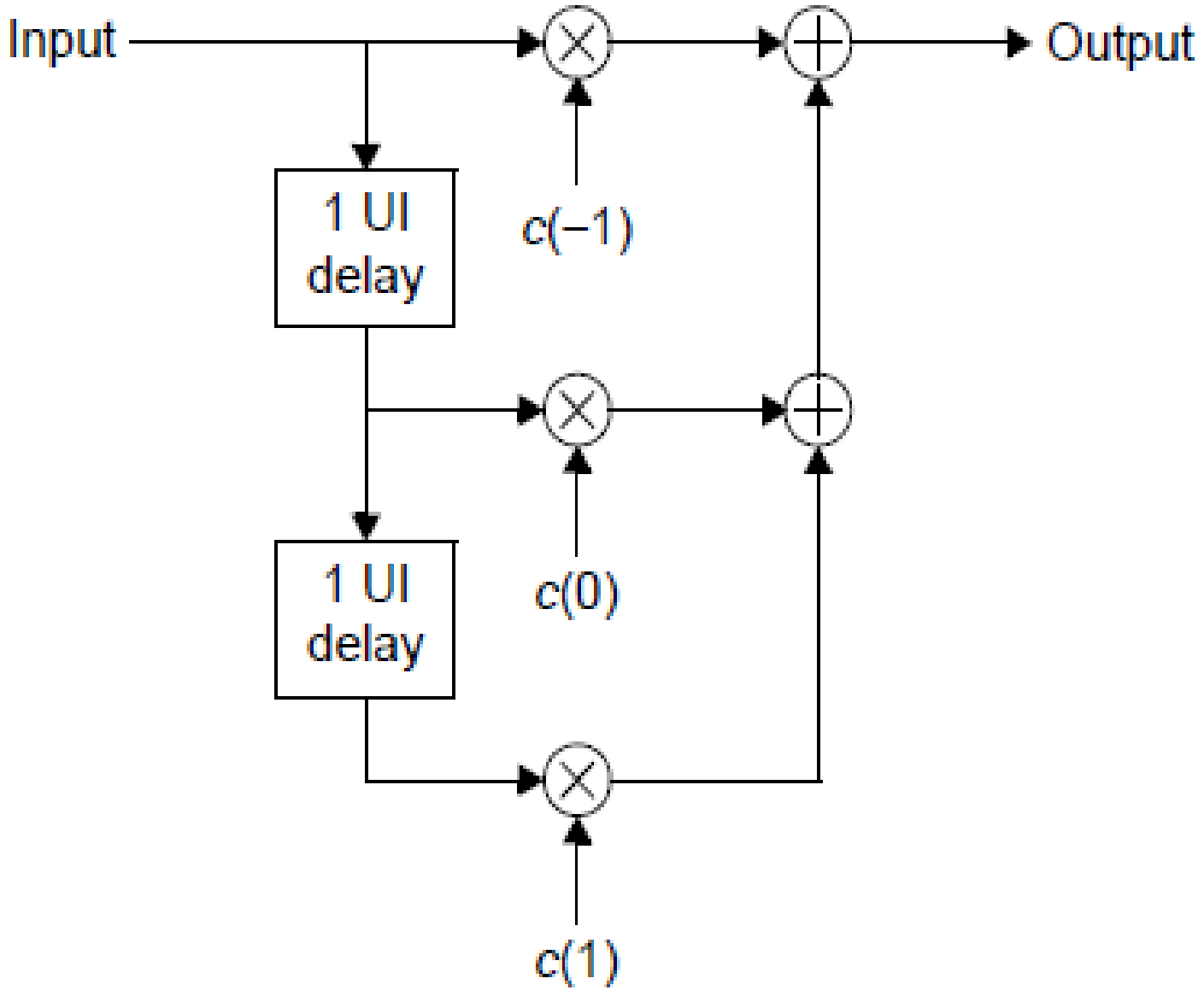

CDAUI-8 chip-to-chip channel insertion loss
Insertion Loss (dB)
Frequency (GHz)
0
-10
-20
-30
-40
-50
-60
0
5
10
15
20
25
30
35
40
45
50
$Insertion\ Loss(f) \leq 1.083 + 2.543\sqrt{f} + 0.761f$
$0.01 \leq f < 50$

Parameter	Reference	Value	Units
Signaling rate per lane (Range)		51.5625 ± 100 ppm	GBd
Differential peak to peak output voltage (max)	93.8.1.3		
Transmitter disabled		30	mV
Transmitter enabled		1200	mV
Common-mode voltage (max)	93.8.1.3	1.9	V
Common-mode voltage (min)	93.8.1.3	0	V
AC common-mode output voltage (mas, RMS)	93.8.1.3	12	mV
Differential output return loss (min)		TBD	dB
Common-mode output return loss (min)		TBD	dB
Output waveform[a]			
Steady state voltage vf (max)	93.8.1.5.2[b]	0.6	V
Steady state voltage vf (min)	93.8.1.5.2[b]	0.4	V
Linear fit pulse peak (min)	93.8.1.5.2[b]	0.71 x v_f	V
Pre-cursor equalization	98D.3.1.1	Table 98D–2	-
Post-cursor equalization	98D.3.1.1	Table 98D–3	-
Signal-to-noise-and-distortion ratio (min)	93.8.1.6[b]	27	dB
Output Jitter (max)	92.8.3.8		
Even-odd jitter		0.035	UI
Effective bounded uncorrelated jitter, peak-to-peak[c]		0.1	UI
Effective total uncorrelated jitter, peak-to-peak[cd]		0.22	UI

[a]The state of the transmit equalizer is controlled by management interface.

[b]The values of the parameters are measured as defined in the referenced subclause except that the values of N_p and N_w are 5.

[c]Effective bounded uncorrelated jitter and effective total uncorrelated jitter are measured as defined in 92.8.3.8.2.



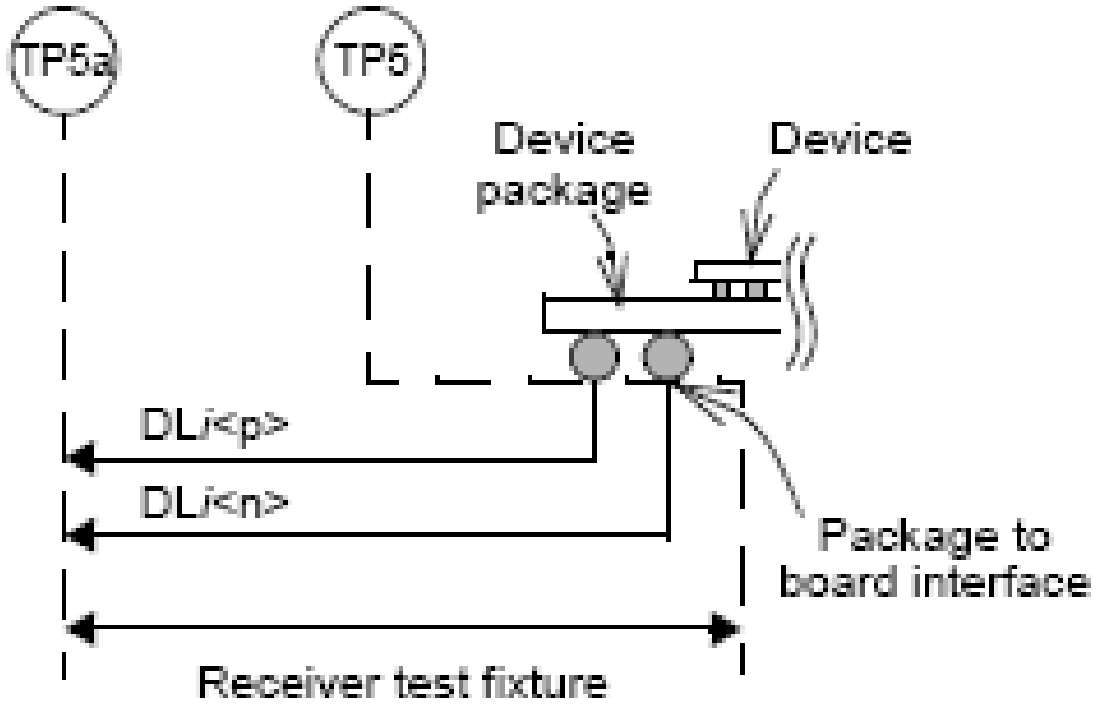
Transmit equalizer functional model

Pre-cursor equalization

Local_eq_cm1 value	$c(-1)$ ratio $\left(\frac{c(-1)}{\lvert c(-1)\rvert + \lvert c(0)\rvert + \lvert c(1)\rvert}\right)$
0	0±0.04
1	-0.05±0.04
2	-0.1±0.04
3	-0.15±0.04

Post-cursor equalization

Local_eq_c1 value	$c(1)$ ratio $\left(\frac{c(1)}{\lvert c(-1)\rvert + \lvert c(0)\rvert + \lvert c(1)\rvert}\right)$
0	0±0.04
1	-0.05±0.04
2	-0.1±0.04
3	-0.15±0.04
4	-0.2±0.04
5	-0.25±0.04



CDAUI-8 receiver compliance points

Receiver interference tolerance parameters

Parameter	Test 1 Values			Test 2 Values			Units
	Min	Max	Target	Min	Max	Target	
Bit error ratio[ab]	-	10^{-6}		-	10^{-6}		-
Applied pk-pk sinusoidal jitter			Table 88-13			Table 88-13	
Insertion loss at 26 GHz[c]	31	32		10	11		dB
Coefficients of fitted insertion loss[d]							
a_0	-1	2		-1			dB
a_1	0	2.937		0.817			$dB/GHz^{1/2}$
a_2	0	1.599		0.801			dB/GHz
a_4	0	0.03		0.01			dB/GHz^2
RSS_DFE2[e]					-		-
COM including effects of broadband noise	-	-	2	-	-	2	dB

[a]Bit error ratio replaces the RS symbol error ratio measurement in 93.8.2.3

[b]Maximum BER assumes errors are not correlated to ensure sufficiently high mean time to false packet acceptance (MTTFPA) assuming 64B/66B coding. Actual implementation of the receiver is beyond the scope of this standard

[c]Measured between TPt and TP5 (see Figure 93C-4)

[d]Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C-4) using the method in 93A.3 with f_{min} = 0.05 GHz, and f_{max} = 51.5625 GHz, and maximum Δf = 0.01 GHz

[e]RSS_DFE2 is equivalent to RSS_DFE4 described in 93A.2 except that n_1=2 and n_2=5.

Channel Operating Margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	51.5625	GBd
Maximum start frequency	F_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model			
Single-ended device capacitance	C_d	2.5×10^{-4}	nF
Transmission line length, Test 1	Z_p	12	mm
Transmission line length, Test 2	Z_p	30	mm
Single-ended board capacitance	C_b	1.8×10^{-4}	nF
Single-ended reference resistance	R_o	50	ohms
Single-ended termination resistance	R_d	55	Ohms
Reciever 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, minimum cursor coefficient	c(0)	0.6	-
Transmitter equalizer, pre-cursor coefficient	c(-1)		-
Minimum value		-0.15	
Maximum value		0	
Step size		0.05	
Transmitter equalizer, post-cursor coefficient	c(1)		-
Minimum value		-0.35	
Maximum value		0	
Step size		0.05	

Continuous time filter, DC gain **Minimum value** **Maximum value** **Step size**	g_{DC}	 **-12** **0** **1**	**dB**
Continuous time filter, zero frequency	f_z	$f_b/4$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b/4$ f_b	GHz
Transmitter differential peak output voltage **Victim** **Far-end aggressor** **Near-end aggressor**	 A_v A_{fe} A_{ne}	 0.4 0.4 0.6	 V V V
Number of signal levels	L	2	-
Level seperation mismatch ratio	R_{LM}	1	
Transmitter signal-to-noise ratio	SNR_{TX}	27	dB
Number of samples per unit interval	M	32	-
Decision feedback equalizer (DFE) length	N_b	5	UI
Normalized DFE coefficient magnitude limit, for n=1 to Nb	$B_{max}(n)$	1.0	-
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.05	UI
One-sided noise spectral density	η_o	5.2×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-6}	-