An Alternative Scheme of FOM Bit Mux with Pre-interleave

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Background

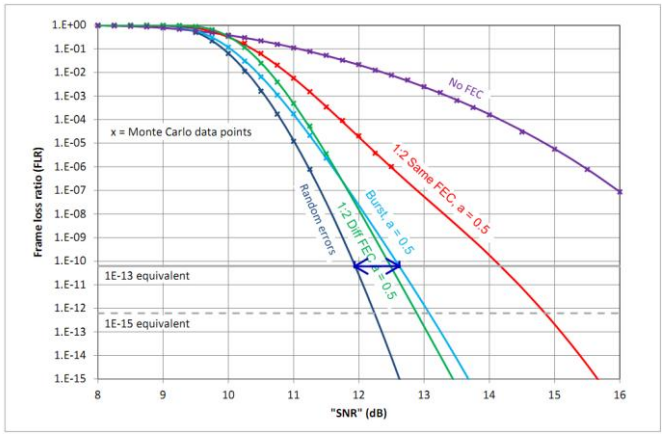
- PMA options as in “gustlin_3bs_04_0714” are:
  - Bit Muxing, used in 802.3ba
  - FEC Orthogonal Multiplexing
  - Block muxing
  - There might be a complex line encoding that has a unique multiplexing method

- In this presentation, we provide an optimized choice of FEC Orthogonal Multiplexing by pre-interleaving to relax the constraints on layout implementation and support any lane to anywhere feature.

Brief Introduction of FOM Bit Mux

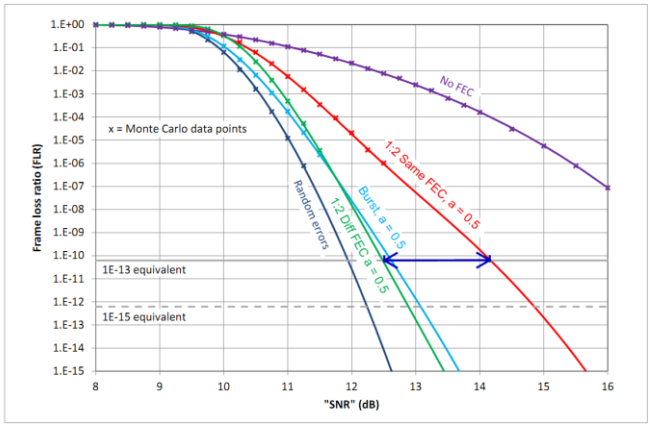
- FEC Orthogonal Multiplexing is a general approach to help FEC performance, it is mature technology and already deployed to face correlate error applications.
- From previous analysis, we can see the improvement of coding gain by FOM symbol mux and FOM bit mux against burst errors.*

RS(528,514) all curves



FOM symbol mux vs. NonFOM symbol mux

RS(528,514) all curves

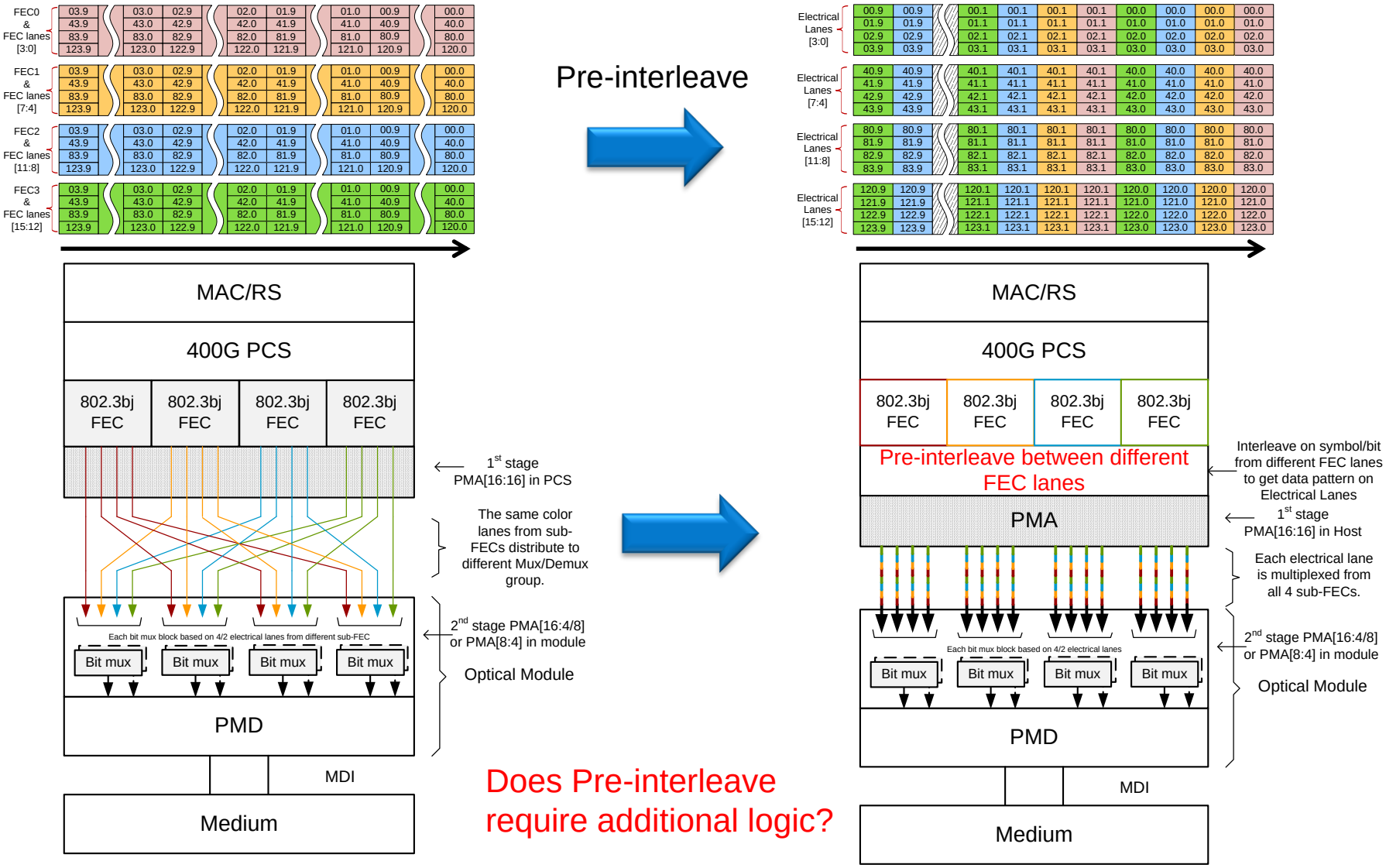


FOM bit mux vs. NonFOM bit mux

- Some concerns raised about FOM for its constraints on layout of CDAUI as stated in "wang_400_01a_0114", although we think implementation with this restriction is feasible.
- Can we have tradeoff between flexibility and performance if any FEC lane to anywhere architecture is preferable?

**refer to anslow_3bs_02_0714*

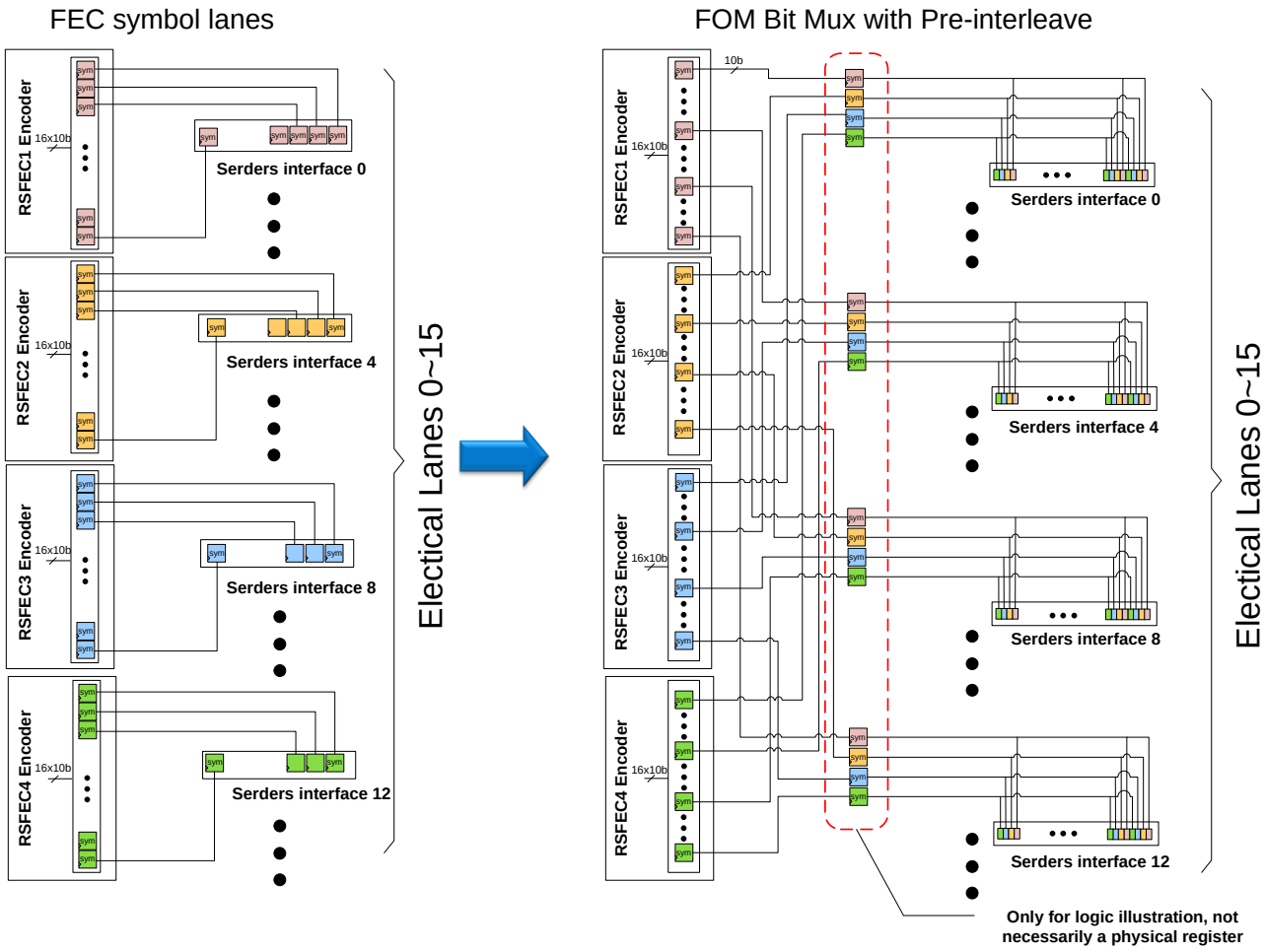
Optimize FOM Bit Mux with Pre-interleave



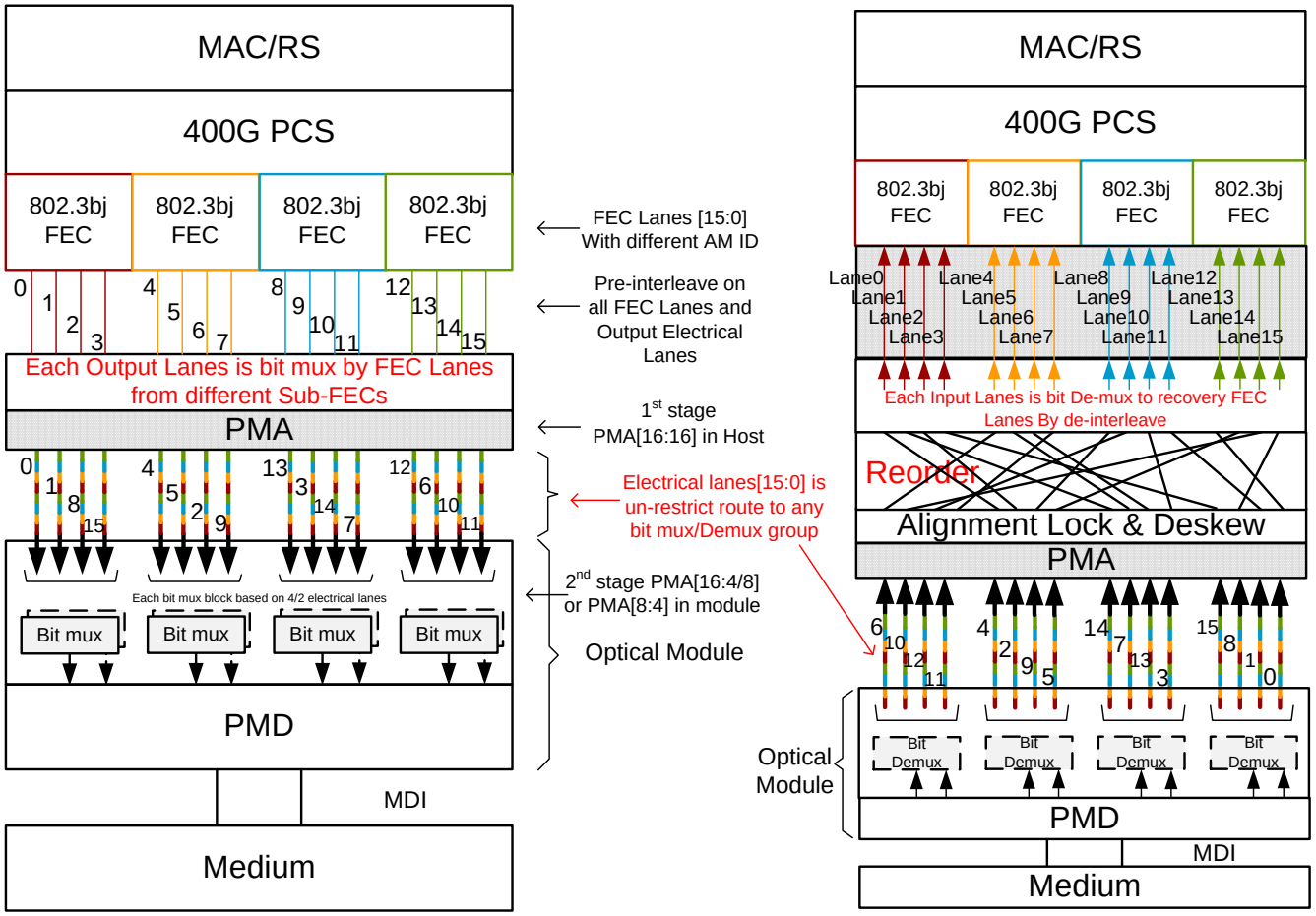
Does Pre-interleave require additional logic?

Hardware Implementation of Pre-interleave

- Take TX logic for example, each FEC encoder output parallel data bus according to 100Gbps throughput.
- It is just different logic place and route option inside host ASIC to feature
  - One FEC Lane to one Serdes interface Or,
  - Symbols from multiple FEC Lanes to one Serdes interface
- No multiplexers involved
  - No additional latency cost
  - No additional area cost
- RX logic procedure is similar and operable on parallel logic.



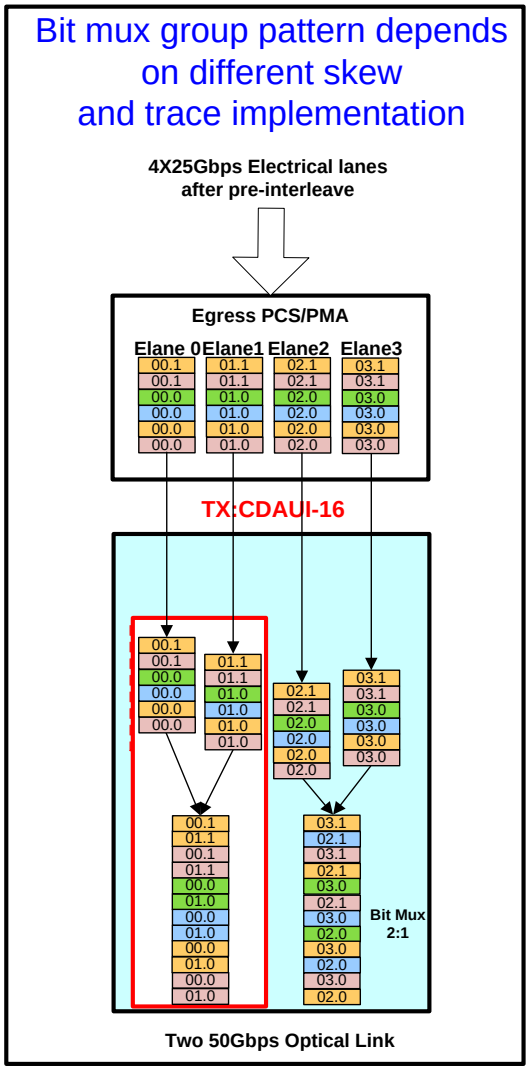
RX Side: Alignment and Reorder Before De-interleave



- Use alignment and reorder mechanism in RX side across all lanes as in 100GE.

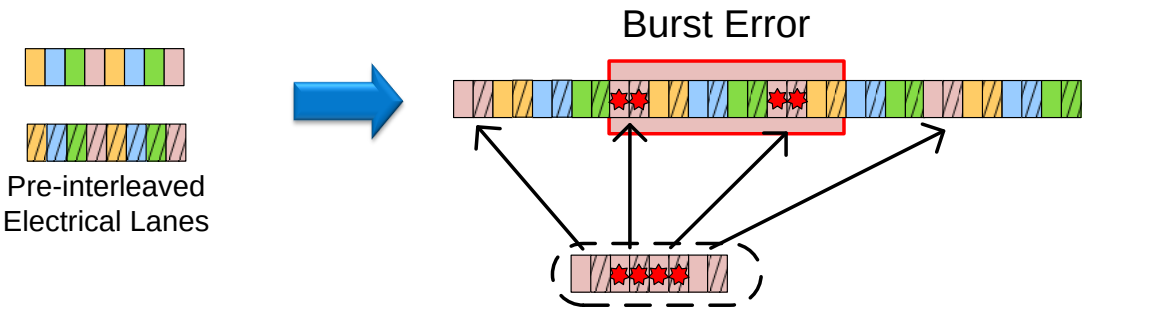
Example: 2:1 Bit Mux with CDAUI-16 interface

- Data stream on16 electrical lanes is bit interleaved from different Sub-FECs by Pre-interleaving.
- Use 16 electrical lanes on CDAUI-16 and multiplex to 50G optical lanes.
- As bit pattern on each electrical lanes is from 4 different sub-FECs, any two electrical lanes can bit-mux together. NO layout restriction on CDAUI interface.
- Use AM Lock/Alignment and Reorder on RX side to restore all FEC lanes before de-interleave;
- The worst case of FEC performance is showed in RED block in right diagram, when bits from same FEC are aligned.



Error Symbol Number and Probability

- Worse case FEC Orthogonal Bit Mux 2:1 with Pre-interleave



- A bl bit burst corrupts x bits on each symbol lane.

$$x = ceil\left(\frac{bl\%8}{8}\right) + floor\left(\frac{bl}{8}\right)$$

- This x corrupted bits cause erroneous symbols as in following equation.

$$Error\ Symbol\ Number = \begin{cases} ceil\left(\frac{x}{m}\right)+1; & of\ \ prob_1 = \frac{\left|x\%m-1\right|}{m} \\ ceil\left(\frac{x}{m}\right); & of\ \ prob_2 = 1-prob_1 \end{cases}$$

- Total number of erroneous symbol is the sum of error symbols from 2 lanes.

$$Error\ Symbol\ Number = error\_number_{lane1} + error\_number_{lane2};\quad of\ \ prob\ = Prob_{lane1} * Prob_{lane2}$$

Comparison of Error Symbol Number and Probability

- Number of erroneous symbols caused by burst errors for different PMA muxing methods are listed.

Table 1: Non FOM bitmux (worst case)

Burst Length (bits)	Erroneous symbols	Probability
2	2	100%
3	3	10%
	2	90%
4	4	1%
	3	18%
	2	81%
5	4	6%
	3	38%
	2	56%
6	4	4%
	3	32%
	2	64%

Table 2: PreInterleave bitmux(worst case)

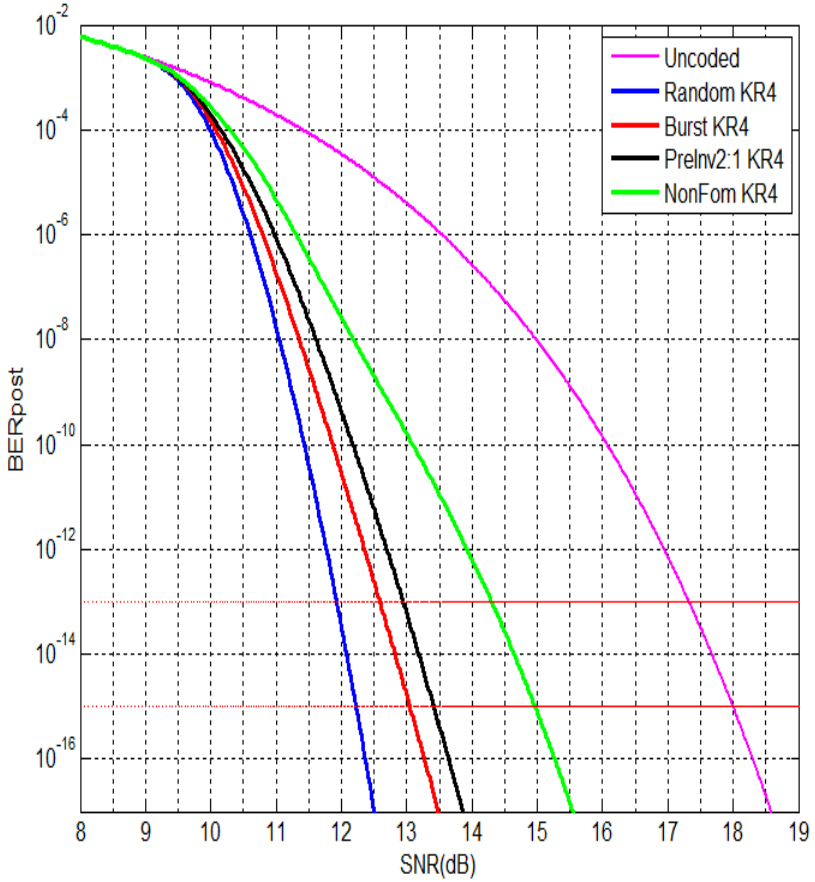
Burst Length (bits)	Erroneous symbols	Probability
2-8	2	100%
9	3	10%
	2	90%
10-16	4	1%
	3	18%
	2	81%
17	4	2%
	3	26%
	2	72%
18-24	4	4%
	3	32%
	2	64%

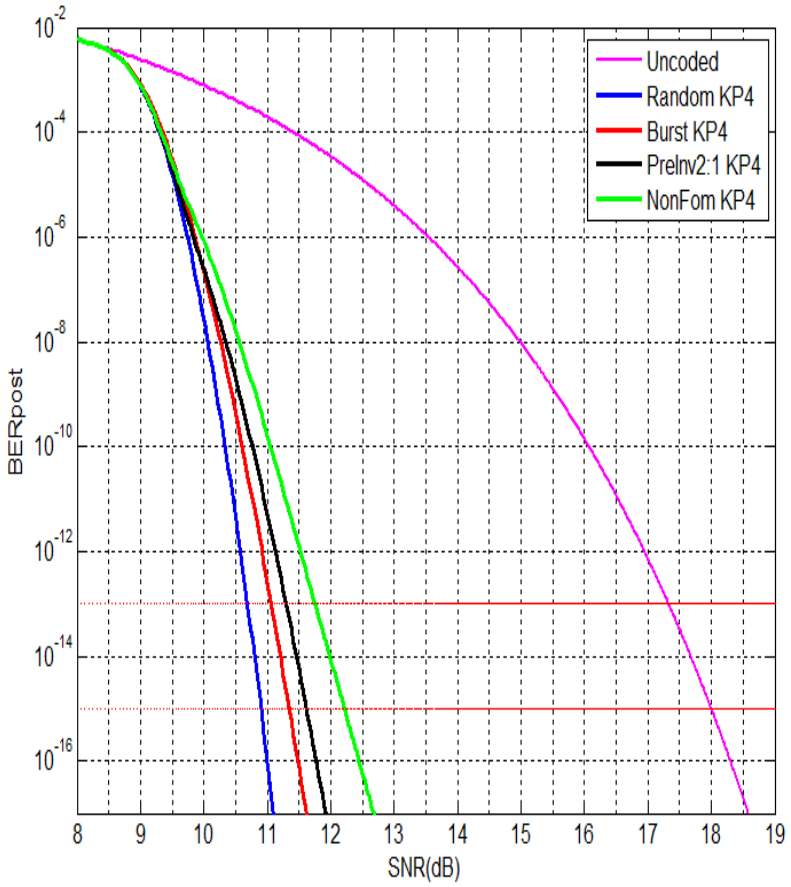
Table 3: FOM bitmux(no worst case)

Burst Length (bits)	Erroneous symbols	Probability
2	1	100%
3	2	5%
	1	95%
4	2	10%
	1	90%
5	2	15%
	1	85%
6	2	20%
	1	80%

- Pre-interleaving method has better resistance of burst errors than NonFOM bitmux(random muxing), but worse than FOM bitmux.
- The advantage of Pre-interleaving method is supporting any lane to anywhere.

FEC performance of FOM 2:1 Bit Mux with Pre-interleave





- FOM bit mux with Pre-interleave require ~0.3dB/0.25db CG Penalty compare to 802.3bj KR4/KP4 FEC in burst error application

Summary

- Pre-interleaving gives another way to do FOM bit mux. It can support any lane to anywhere routing with compromised coding gain.
- We have tradeoff between FEC performance and flexibility for FOM bit mux.
- For BER objective 1e-13

	RS(528,514)		RS(544,514)		Any to any conncetion
	Coding Gain	BERin	Coding Gain	BERin	
Random Errors	5.4	4.00E-05	6.64	3.00E-04	Yes
1:2 FOM symbol mux	5.4	4.00E-05	6.64	3.00E-04	No, Partial lane order required
1:2 FOM bit mux	5.3	1.90E-05	6.34	2.00E-04	No, Partial lane order required
1:2 NON FOM symbol mux	4.7	1.40E-05	6.26	2.40E-04	Yes, as .bj
1:2 FOM bit mux with Pre-interleave	4.4	5.00E-06	6.02	1.20E-04	Yes
1:2 NON FOM bit Mux	3	3.50E-07	5.57	5.50E-05	Yes

- Gray coding in PAM4 could limit correlated error to one bit per PAM4 symbol and help to improve FEC performance in bit mux. We will investigate it in the future.

Thank you