OIF's CEI-XSR-56G-NRZ A CANDIDATE C2EO CDAUI-8

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Introduction

- "Proposal for LPPI"* proposes a C2EO or LPPI, with 50 mm or 2.0" reach across a PCB, with ball-to-ball insertion loss of 4 dB at 14 GHz or 8 dB at 28 GHz. This could be used as a PMD service interface
  - It is distinct from the higher loss C2M and C2C CDAUI-8
- Slide 12 of "Big Ticket Items"† has actions for LPPI:
  - C2C and C2M interaction across the 3 reaches
  - Refine proposal and build consensus
- This presentation describes a suitable specification whose development is well under way, that could be used to refine the LPPI proposal

* http://ieee802.org/3/bs/public/14_11/goergen_3bs_02_1114.pdf

† http://ieee802.org/3/bs/public/15_01/big_ticket_items_3bs_01_0115.pdf

More references on slide 11

Motivation

- An chip-to-chip interface operating at 39-57.8 Gbps that is optimized for **minimum power** consumption, to facilitate an efficient interface to a board mounted optical engine
- 8 dB insertion loss at 28.9 GHz (5 to 7 cm of current generation PCB materials)
  - To allow much higher face-plate optical densities compared to using modules
  - To allow lower power for the same bit rate compared to using modules
  - Be forward looking when newer PCB materials allow a 10 to 12 cm reach for an 8 dB insertion loss, for lower module interface power
- Also for an efficient interface to a separate backplane driver IC
  - i.e. to a "shim" chip, which fulfils a similar function to an optical engine
- Also can be used for low pin count memory interface

The CEI-56G family

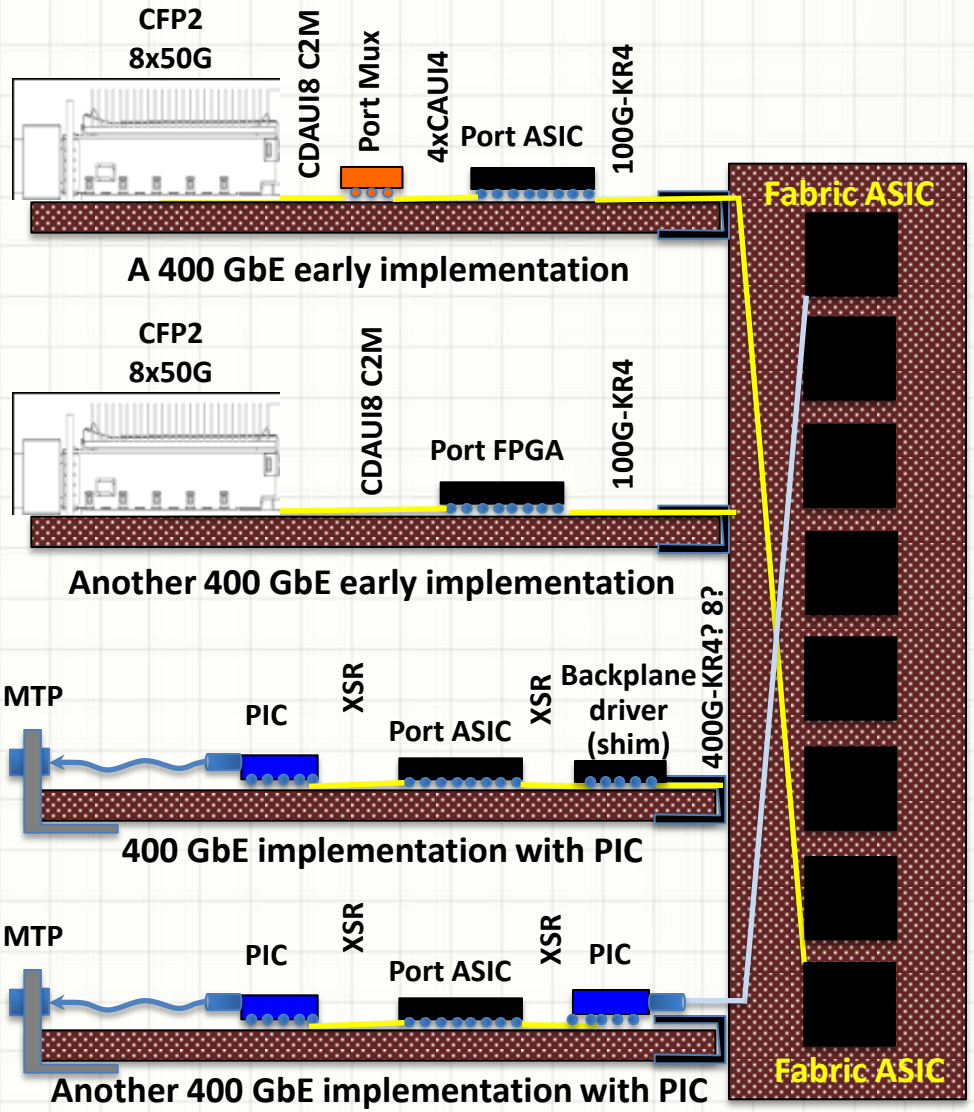
OIF	802.3bs equivalent	Coding	Loss @ 15 GHz	Loss @ 28 GHz	Length (cm)	Connectors	Relies on FEC?
USR		NRZ	-	2	1	None	No
XSR	Chip-to-EO CDAUI-8 or "LPPI*"	NRZ	-	8	5-7	None	No
		PAM4	4.25	-	5		
VSR	C2M CDAUI-8	NRZ	-	15-18	10-15	1	Optional
		PAM4	11	-	15		Yes
MR	C2C CDAUI-8	NRZ	-	~38	50	Up to 1	Yes
		PAM4	20	-			
LR		TBD	35 dB at 14	-	"full-sized backplane"	Up to 2	Likely

* Proposal for LPPI, goergen_3bs_02_1114 (showing an unretimed interface like nPPI)

- All members of the OIF CEI-56G family assume retiming at either end
- XSR and USR use radically lower power clocking arrangements than the others
- See slide 11 for more references

400 GbE capable systems

- **Systems based on CFP2 (8x50G) will deliver the same capacity as QSFP28 linecards (3.2-3.6 Tb/s)**
  - CFP2 belly to belly is not viable for blade systems
- **400 GbE implementations based on board mounted optical engine (PICs) could double the line card capacity to 6.4 Tb/s**



Comparing with other links

- 56G-XSR-NRZ / CDAUI C2EO or LPPI (5-7 cm):
  - 8 dB @ 28 GHz, no connector, no caps
    - Newer materials (Tachyon/Meg7) getting close to 10-12 cm
  - No Tx Emphasis required, 300 to 400 mVppd launch
    - Lower power/area
  - Common clock (sync), no clock recovery (simpler ϕ recovery)
    - Removes jitter tolerance testing, some power/area saving
  - 10^{-15} BER without FEC
    - Lower power/latency/area compared to links that require FEC
  - Fixed CTLE
    - Lower power/area compared to links that require adaptable CTLE
- 56G-VSR / CDAUI C2M (10-15cm)
  - NRZ: 15-18 dB @ 28 GHz, FEC optional to get 10^{-15} BER
  - PAM4: 11 dB @ 15 GHz, FEC required to get 10^{-15} BER
  - Connector + caps required
  - Async ➔clock recovery
  - Tx emphasis likely needed, ~600/800 to 900 mVppd launch
  - Adaptable CTLE required

56G XSR vs. VSR

	XSR		VSR		
Modulation	**NRZ**	**PAM4**	**NRZ**		**PAM4**
Common reference clock	Yes, 1/64	No	No		
Needs FEC? BER	No, spec 1e-15, measure 1e-12		No	Yes	Yes, 1e-6 pre FEC
Tx Vpkpk	300 to 400	400 to 600	600 to 900		800 to 900
Tx emphasis	No		Unspecified		
Connector	No		Yes		
Coupling	DC		AC		
Rx equaliser	Unspecified		Yes e.g. CTLE and DFE	Yes e.g. CTLE	Yes e.g. CTLE

- Aggressive simplification for reduced power consumption on the left

CEI-XSR-56G-NRZ status

- Finished second straw ballot
  - First ballot had 44 technical comments
    - Several big ticket items were resolved
  - Second ballot had 32 technical comments
    - Single big ticket item left to be resolved
      - The common clock architecture
- Next OIF meeting is 20-24 Apr
- Principal Member ballot likely Q1 2016

Summary

- XSR (LPPI/CDAUI C2EO) is an optimized-power link intended for up to 8 dB of channel loss
  - Quite different from VSR (CDAUI C2M)
- Minimum power is essential, therefore NRZ, no equalizers, almost no clock recovery
- XSR's place relates to card architectures, ASIC design and whether any future backplane Ethernet SerDes can fit in the ASIC
- CEI-XSR-56G-NRZ is a very good candidate for a very low power CDAUI-8 for chip-to-optical engine or chip-to-shim use
- Can be used to refine the "Proposal for LPPI"

References

- Joel Goergen and Vasu Parthasarathy, Proposal for LPPI, http://ieee802.org/3/bs/public/14_11/goergen_3bs_02_1114.pdf
- Big Ticket Items for P802.3bs, January 2015 Interim Meeting, http://ieee802.org/3/bs/public/15_01/big_ticket_items_3bs_01_0115.pdf
- CEI-56G-USR oif2014.267.03
- CEI-56G-XSR-NRZ oif2014.268.03
- CEI-56G-XSR-PAM4 oif2014.286.05
- CEI-56G-VSR-NRZ oif2014.277.03
- CEI-56G-VSR-PAM4 oif2014.230.02
- CEI-56G-MR-PAM4 oif2014.245.02
- CEI-56G-MR-NRZ oif2015.053.01
- All the above will be provided to P802.3bs by liaison. Six previous drafts oif2014.267.02, oif2014.268.02, oif2014.286.04, oif2014.277.02, oif2014.230.01 and oif2014.245.01 are available from http://ieee802.org/3/minutes/nov14/index.html and http://ieee802.org/3/bs/private/index.html
- OIF-CEI-03.1, Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps and 25G+ bps I/O, http://www.oiforum.com/public/documents/OIF_CEI_03.1.pdf

QUESTIONS?