Baseline Proposal for CDAUI-8 Chip-to-Chip (c2c)

For IEEE 802.3bs

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* Changes since *li_3bs_01_0115* shown in red

Purposes

- Present a PAM4 baseline specification proposal for CDAUI-8 c2c electrical interface in support of the 400 GbE to fulfill its objective of:

  Support optional 400 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications

Technology Choice Highlights 1

- Channel target/requirement based on the equation of the following:
  - IL <= { 1.083 + 2.543SQROOT(f) + 0.761f 0.01 <= f <= 28.05GHz} dB

  as the informative insertion loss equation adopted by 802.3bs in Jan/2015 meeting
- Channel equalization based on a transceiver having TX FIR, RX CTLE and DFE

Technology Choice Highlights 2

- Raw BER of CDAUI-8 link to be < 1E-6; FEC brings link system BER to < 1E-15

Technology Choice Highlights 3

- Leverage the 100GBASE-KP4 (i.e., KP4) specification from 13.59 GBd to 26.5625 GBd, and is consistent with CEI-56G-MR specification draft[1]
- Gray-code proposed, FEC (capable of bringing raw BER from 1e-6 to < 1e-15) assumed. FEC and pre-coding (if needed) specifics be defined by the FEC ad hoc
- Reuse KP4 test patterns, TX and RX methodologies for specifying electrical characteristics and corresponding tests
- Reuse CAUI-4 TX and RX diff and CM RLs, compliance point definitions (i.e., TP0a and TP5a)
- Reuse CAUI-4 link adaptation method (i.e., CL 83D.3.3.2 and 45)
- Reuse/improve 802.3bj COM method channel compliance with PAM4 signaling

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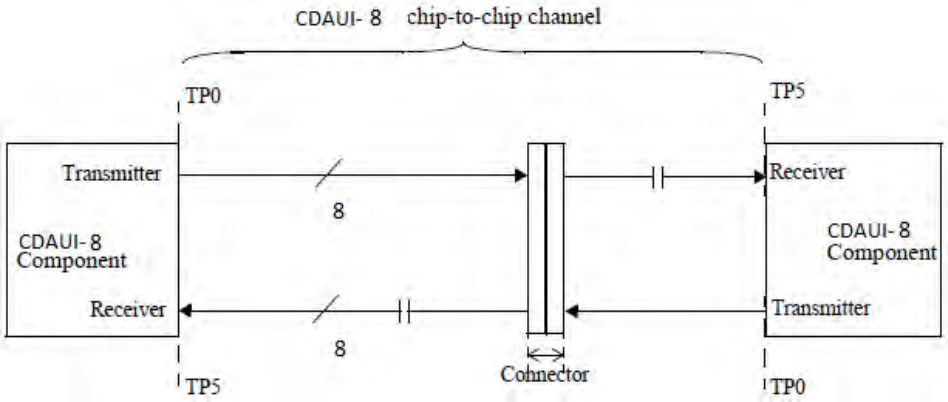
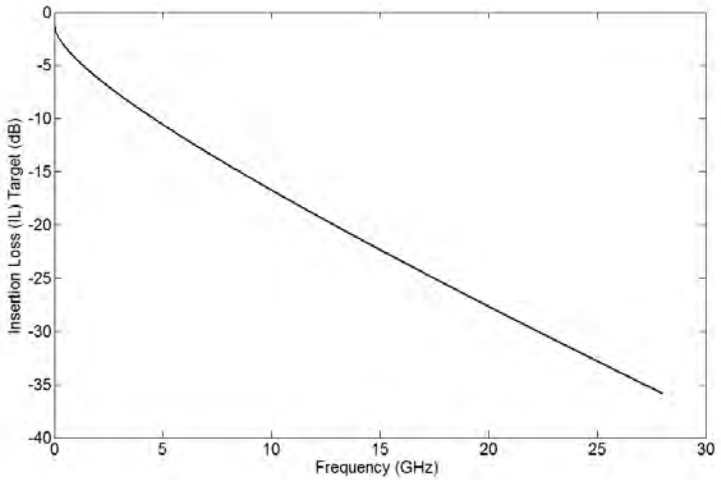
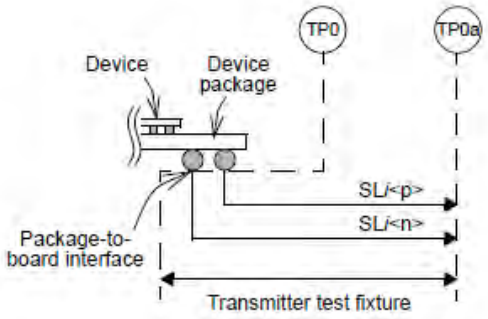
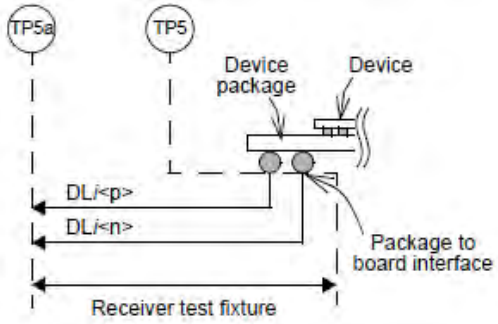
CDAUI-8 c2c Link Topology and IL Target



Informative target Max IL







- CDAUI-8 c2c compliance point definitions are the same as those defined in clause 83D.2 (CAUI-4)

CDAUI-8 c2c Functional Spec

- CDAUI-8 PMA functional spec will be largely base on reusing, extending/modifying Clauses 94.2.2 (TX), 94.2.3 (RX), including
  - FEC interface
    - KP4 FEC, i.e., RS(544, 514, 10)
  - Gray mapping
  - PAM4 encoding
  - Precoding
    - Pending, the need and specifics ought to be studied and determined in the FEC ad hoc

CDAUI-8 c2c Test Patterns

- CDAUI-8 PMA will reuse test patterns defined in clause 94.2.9, including:
  - JP03A test pattern
  - JP03B test pattern
  - Quaternary PRBS13 test pattern (with the termination block (i.e., 94.2.2.4) removed, this will need to be changed accordingly)
  - Transmitter linearity test pattern

CDAUI-8 c2c TX Spec

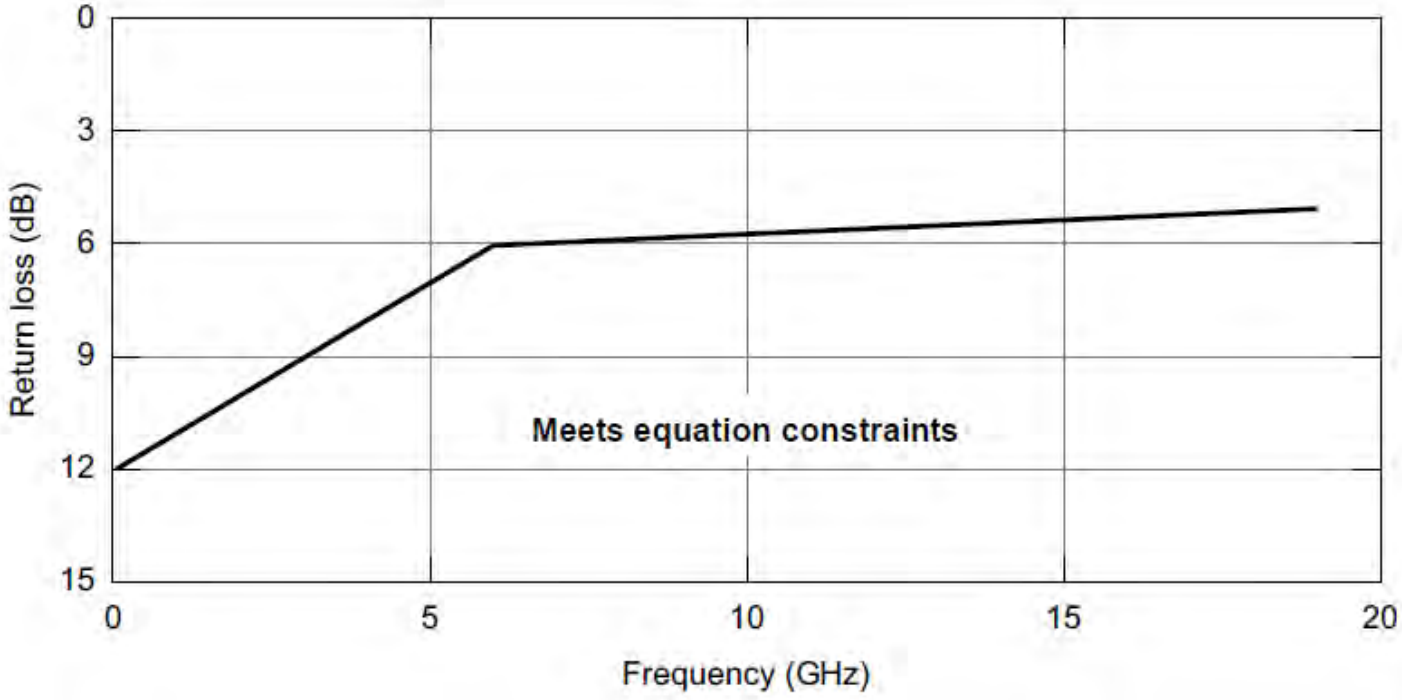
Parameter	Subclause reference	Value	Units
Signaling rate		26.5625	Gsym/s
Differential peak-to-peak output voltage (max.) Transmitter disabled Transmitter enabled		 30 1200	 mV mV
DC common-mode output voltage (max.)		1.9	V
DC common-mode output voltage (min.)		0	V
AC common-mode output voltage (RMS, max.)		30	mV
Differential output return loss (min.)		Eq. 17-4	dB
Common-mode output return loss (min.)		Eq. 17-5	dB
Output waveform Level separation mismatch ratio RLM(min) Steady-state voltage v_f (max.) Steady-state voltage v_f (min.) Linear fit pulse peak (min.) Normalized coefficient step size (min.) Normalized coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)		 0.92 0.6 0.4 0.80 × v_f 0.0083 0.05 1.54 4	 — V V V — — — —
Output jitter and linearity Clock random jitter, RMS (max.) Clock deterministic jitter, pp (max.) Even-odd jitter (max.) Signal-to-noise-and-distortion ratio (min.)		 0.01 0.04 0.019 31	 UI UI UI dB

- TX output waveform definition and test method will reuse clause 94.3.12.5
- TX output jitter definition and test method will reuse clause 94.3.12.6
- TX output noise and distortion definition and test method will reuse clause 94.3.12.7

* Updated to be aligned/consistent with *healey_3bs_01_0315*

CDAUI-8 c2c TX Diff RL Spec

$$RL_d(f) \geq \begin{cases} 12.05 - f & 0.05 \leq f \leq 6 \\ 6.5 - 0.075f & 6 < f \leq 19 \end{cases} \text{ dB}$$



- Reuse Eq. (93-3) and Fig (93-7)

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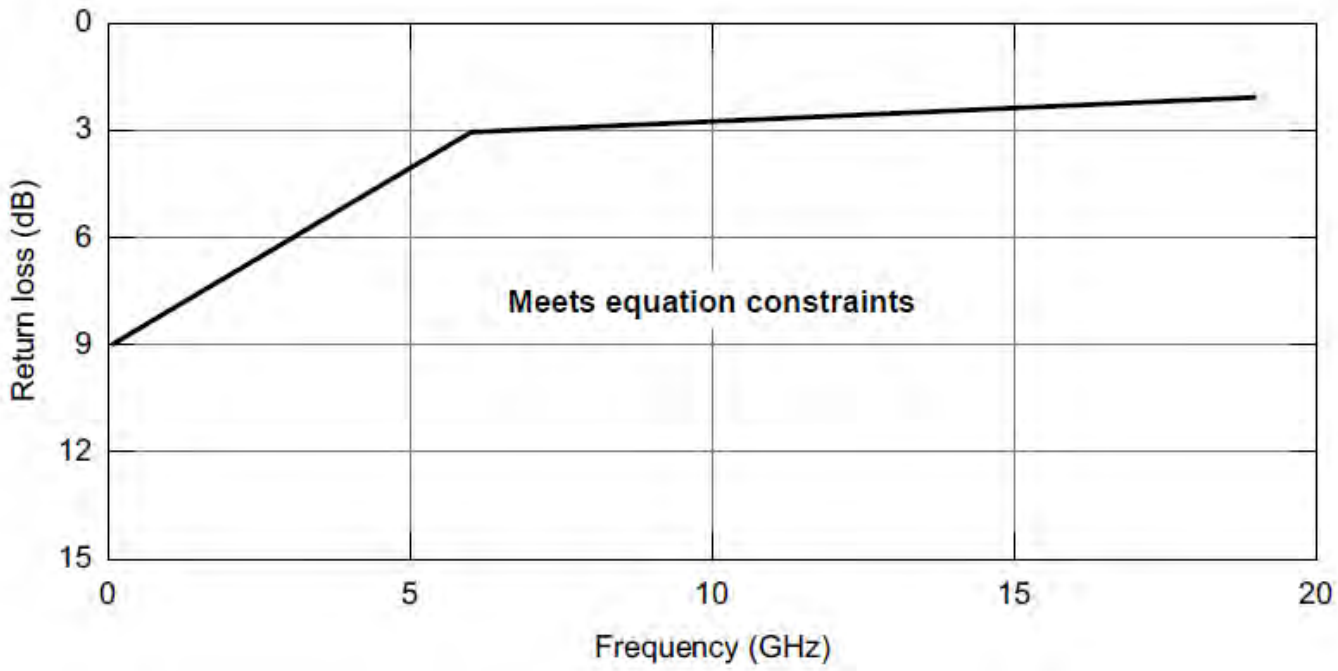
CDAUI-8 c2c TX CM RL Spec

$$RL_{cm}(f) \geq \begin{cases} 9.05 - f & 0.05 \leq f \leq 6 \\ 3.5 - 0.075f & 6 < f \leq 19 \end{cases} \text{ dB}$$



- Reuse Eq. (93-4) and Fig (93-8)

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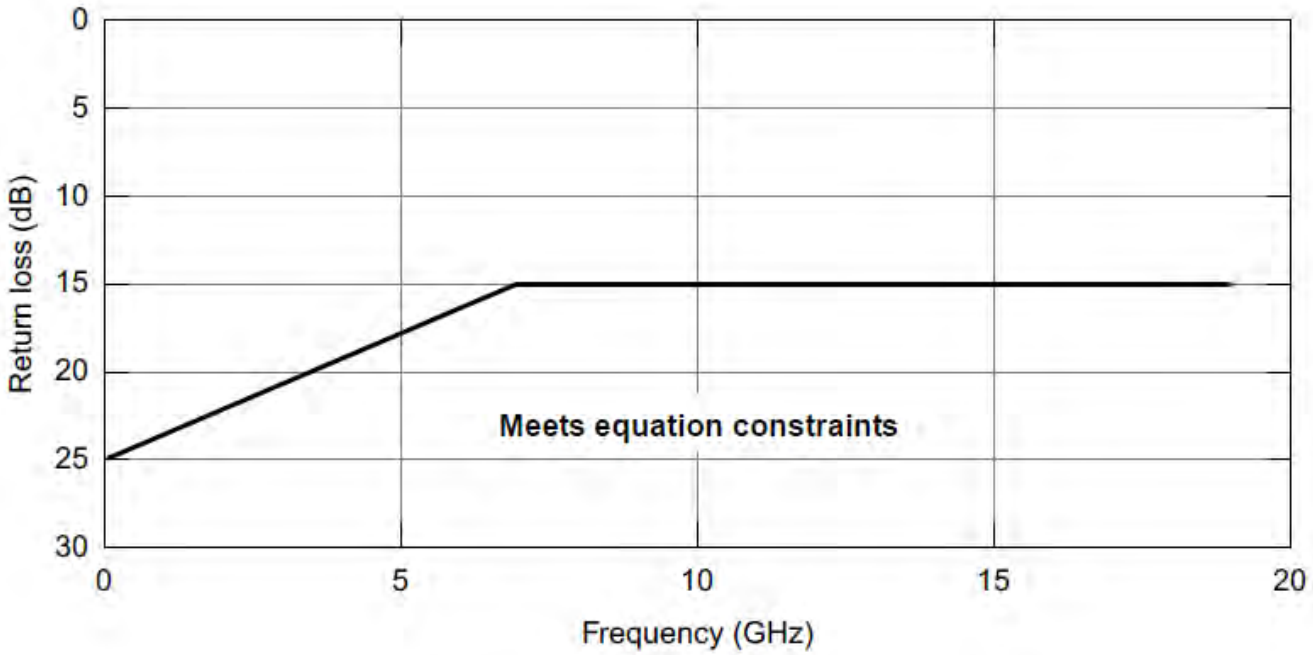
CDAUI-8 c2c RX Spec

Parameter	Symbol	Value	Units	Conditions
Differential Input Return Loss		Slide 11	dB	
Differential to Common-Mode Return Loss		Slide 14	dB	
Interference Tolerance		Slide 15	-	
Jitter Tolerance		Slide 16	-	

CDAUI-8 c2c RX D2C RL Spec

$$RL_{cd}(f) = \left\{ \begin{array}{ll} 25 - 1.44f & 0.05 \le f \le 6.95 \\ 15 & 6.95 < f \le 19 \end{array} \right\} \text{ dB}$$



- Reuse Eq. (93-5) and Fig (93-11)

CDAUI-8 c2c RX Interference Tolerance Parameters

Parameter	Test 1 values			Test 2 values			Units
	Min	Max	Target	Min	Max	Target	
Symbol error ratio[a]	—	10^{-5}		—	10^{-5}		—
Insertion loss at 13.2813 GHz [b]	19.5	20.5		9.5	10.5		dB
Coefficients of fitted insertion loss [c] a0 a1 a2 a4	 −1 0 0 0	 2 2.937 1.599 0.03		 −1 0 0 0	 1 0.817 0.801 0.01		 dB dB/GHz $^{1/2}$ dB/GHz dB/GHz ^{2}
RSS_DFE4 [d]	0.05	—		0.025	—		—
COM including effects of broad- band noise	—	—	2	—	—	2	dB

[a] The FEC symbol error ratio is measured in step 11 of the receiver interference tolerance method defined in 93C.2

[b] Measured between TPt and TP5 (see Figure 93C-4)

[c] Coefficients are calculated from the insertion loss measured between TPt and TP5 (see Figure 93C-4) using the method in 93A.3 with fmin = 0.05 GHz, and fmax = 26.5625. GHz, and maximum Δf = 0.01 GHz

[d] RSS_DFE4 is described in 93A.2.

- Largely re-use of Table 83D-5 and method in 94.3.13.3

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CDAUI-8 c2c RX Jitter Tolerance Parameters

Parameter	Case A values	Case B values	Units
Max Pre-FEC BER	1e-6	1e-6	
Jitter frequency	fb/849600	fb/8496	same as fb
Jitter Amplitude	5	0.05	UI

- Largely re-use method in 94.3.13.4
- fb is the BAUD rate

CDAUI-8 c2c Channel Spec: COM (I)*

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended package capacitance at package-to-board interface	 C_d z_p z_R C_p	 TBD 12 30 TBD	 nF mm mm nF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	TBD	Ω
Receiver 3 dB bandwidth	f_r	0.75 × f_b	
Transmitter equalizer, minimum cursor coefficient	$c(0)$	0.60	—
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.15 0 0.05	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.25 0 0.05	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –15 0 1	 dB dB dB
Continuous time filter, zero frequency	f_z	f_b / 4	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	f_b / 4 f_b	GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.4 0.4 0.6	 V V V

* Updated to be aligned/consistent with *healey_3bs_01_0315*

CDAUI-8 c2c Channel Spec: COM (II)

Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.92	—
Transmitter signal-to-noise ratio	SNR_{TX}	31	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	5	UI
Normalized DFE coefficient magnitude limit for n = 1 for n = 2 to N_b	$b_{max}(n)$	1 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	5.2×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-6}	—

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Summary

- A baseline proposal based PAM4 signaling for CDAUI-8 c2c electrical interface specification has been developed
  - Intent is to support existing CAUI-4 c2c channel and testing infrastructures
  - Reused/extended/modified from 100GBase-KP4 and CAUI-4 c2c specifications (i.e., clauses 94, 93A, and 83D)
  - Consistent with CEI-56G-MR adopted baseline specification in modulation and in general

References

[1] oif2014.245.01, www.oiforum.com

(That document was provided as an attachment to the October 28, 2014 liaison from OIF to IEEE 802.3. The liaison and its attachments can be found in the IEEE P802.3bs 400 Gb/s Ethernet Task Force private area)