PAM4 RESULTS FOR COPPER CHANNELS

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CONTRIBUTORS & SUPPORTERS

CONTRIBUTORS

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SUPPORTERS

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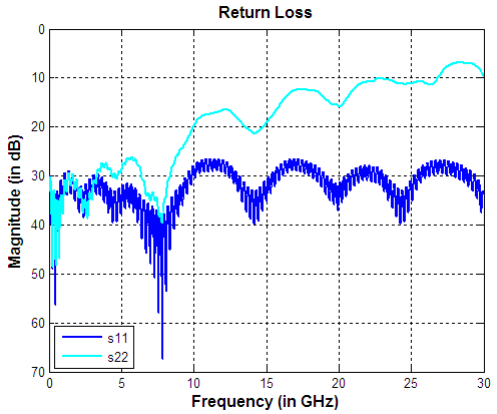
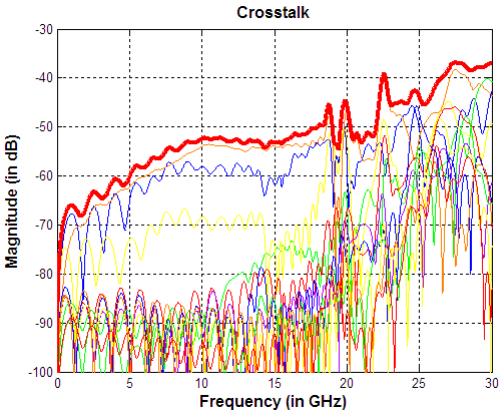
INTRODUCTION

- **PAM4 Simulation results: What we have said so far**
  - Summary on VSR and MR channels
- **Demos: What we have shown so far**
  - Summary of test chip demos on copper and backplane
- **Power projections**
- **Conclusions**

VSR CHANNEL (REF. DOMB_3BS_01A_0714.PDF)

- **Channel**
  - VSR Channel
  - OIF 2014.142.00 (56G VSR)
  - IL: 9.1dB loss @14GHz
  - XT: 11 FEXT, 0 NEXT





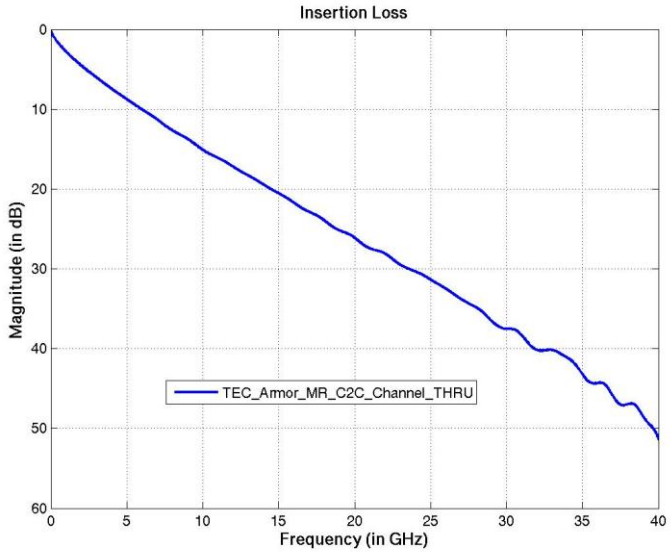
- **Simulation setup**
  - Signaling: 50Gbps, PAM4 ➔ 25.78125GBd
- **Architecture**
  - Tx FIR + CTLE (no DFE)
  - No FEC
- **BER: $1x10^{-25}$**

MR CHANNEL (REF. VALLIAPPAN_3BS_01A_1114.PDF)

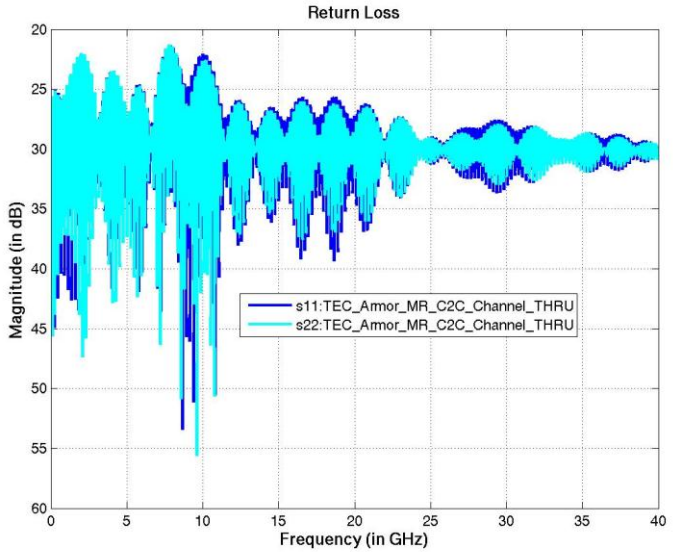
- **Channel**
  - Medium Reach, Chip to Chip channel
  - http://ieee802.org/3/bs/public/channel/TEC/shanbhag_02_0914.pdf (30-Sep-14)
  - IL: 18.2dB @12.9GHz
  - XT: 7 FEXT, 0 NEXT
- **Simulation setup**
  - Signaling: 50Gbps, PAM4 ➔ 25.78125GBd
- **Architecture**
  - Tx FIR + CTLE (no DFE)

MR CHANNEL PARAMETERS

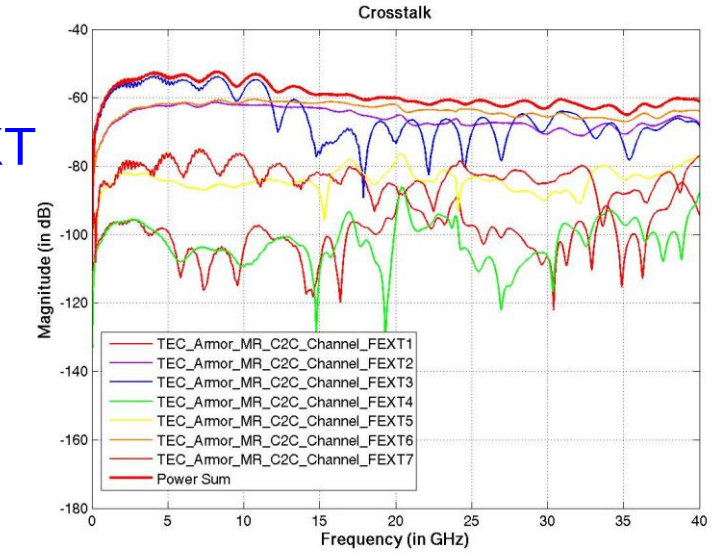
Channel IL



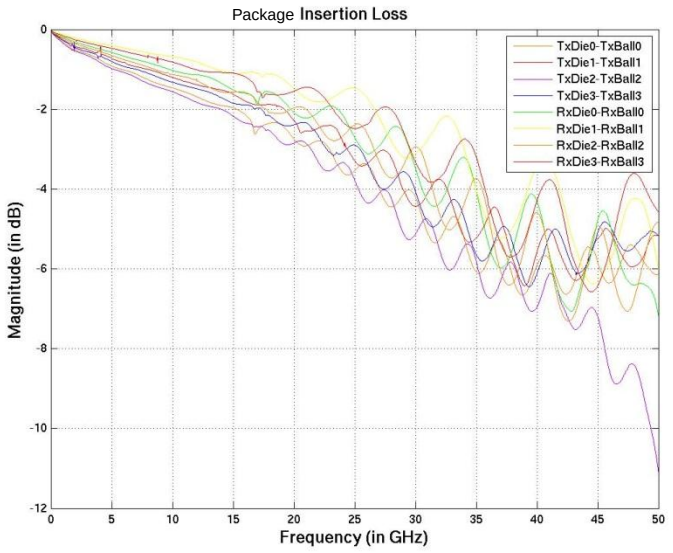
Channel RL



Channel XT



Package IL



MR CHANNEL RESULTS

Metric	Value
BER (pre-FEC)	**$1.4x10^{-10}$**
Vertical EO @ 1e-6	**50mVpp**
Horizontal EO @ 1e-6	**95mUIpp**

- **Sufficient BER to reach error free performance after simple FEC**
- **IEEE 802.3bj 100GBASE-KR4 FEC has no overhead and ~5.6 dB net coding gain (random errors)**
- **With >5 dB of coding gain, BER < 1e-27**

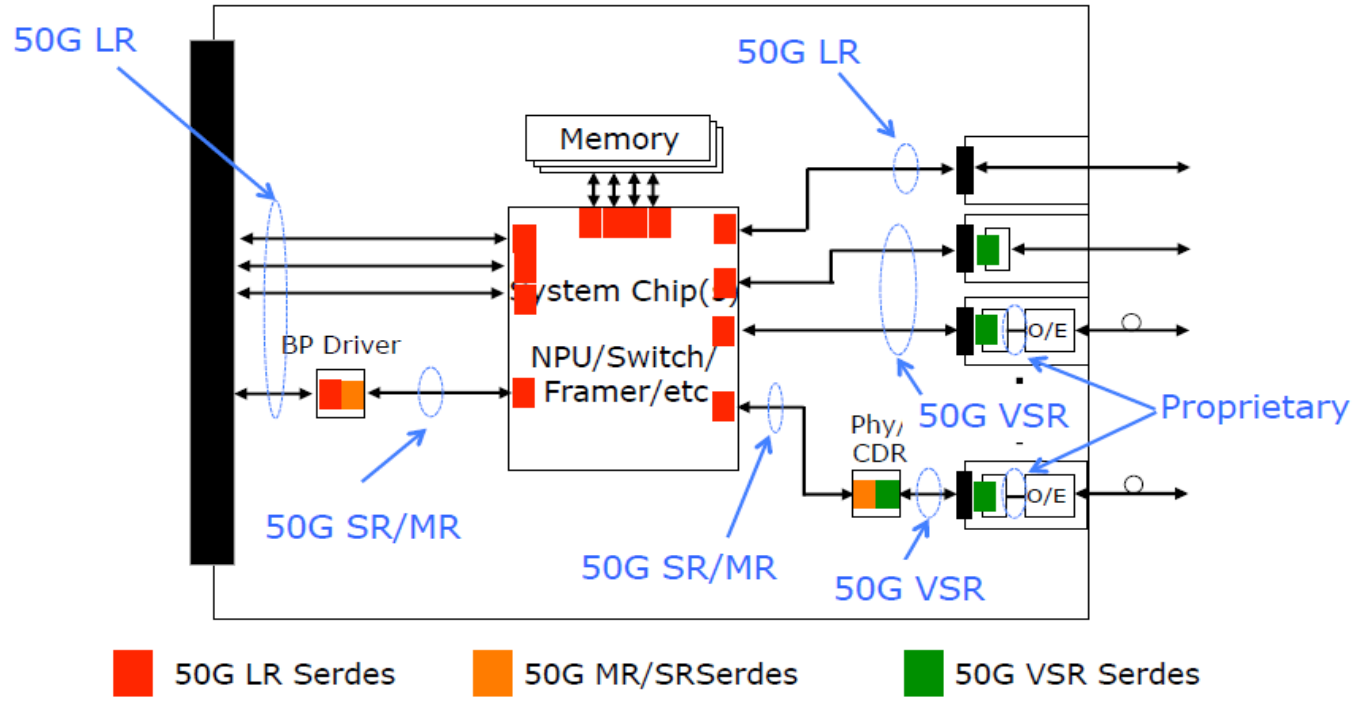
PAM4: MODULATION FOR MULTIPLE REACHES

SINGLE MODULATION FOR MULTIPLE SERDES TYPES: RECAP FROM JANUARY PRESENTATION

“Value of a Common Electrical Modulation Scheme for CDAUI- from a System Perspective”: Gary Nicholl et. al, IEEE Jan 2015, Slide 8

http://www.ieee802.org/3/bs/public/15_01/nicholl_3bs_01c_0115.pdf

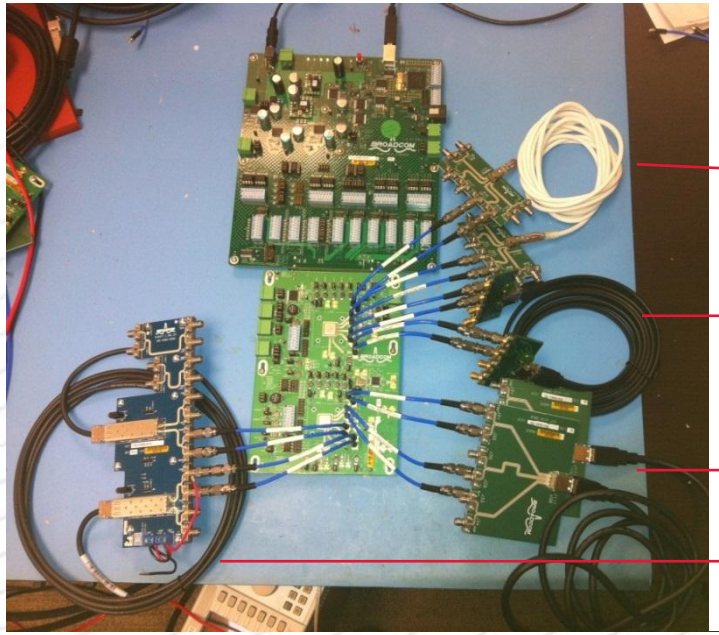
How does this map to 50G Electrical ?



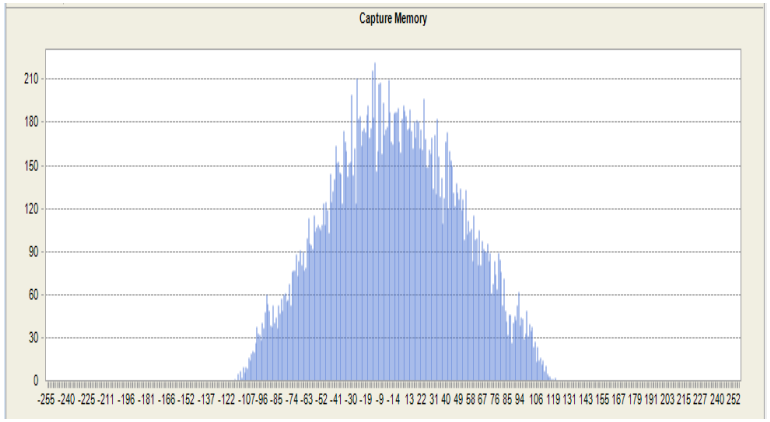
- Switch chip again wants to connect to multiple other serdes type
- More challenging if different modulation used for different interfaces ?

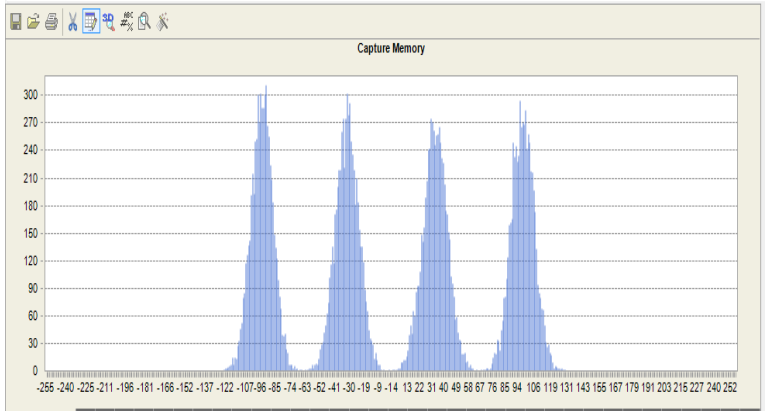
PAM4 TEST CHIP RESULTS: LIVE DEMO IN OFC 2014 (32 GBPS)

- **eSATA, Thunderbolt, USB, CX1 cables bought in open market**
  - Commonly used SerDes media in networking and consumer electronics
  - Error free performance over long runs (overnight)
- **High bandwidth over low-cost medium**
- **Leverage existing connector/cable infrastructure**
- **Higher data throughput over legacy low bandwidth channels**
- **Transfer more bits per symbol at lower cost**



PAM4 Input and Equalized Data Histograms at 32 Gbps (Thunderbolt)





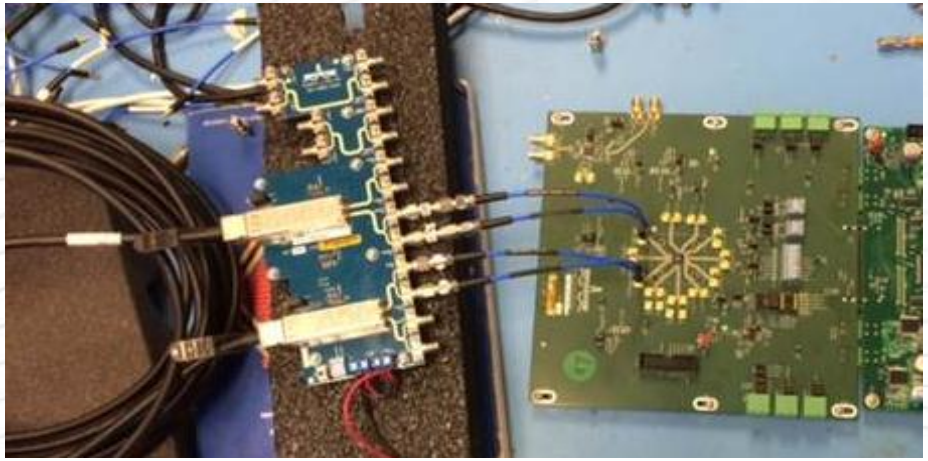
DESIGNCON 2015 LIVE DEMOS (40 AND 50 GBPS)

- **40G PAM4**
  - 40G PAM4 demo: error-free operation on **10m passive TE QSFP cable** (40 Gbps over a single pair)
  - ~30dB insertion loss at PAM4 Nyquist, crosstalk (NOTE: NRZ Nyquist is 55-60 dB!!)
  - No external intervention – equalization, adaptation, FEC, are all on-chip

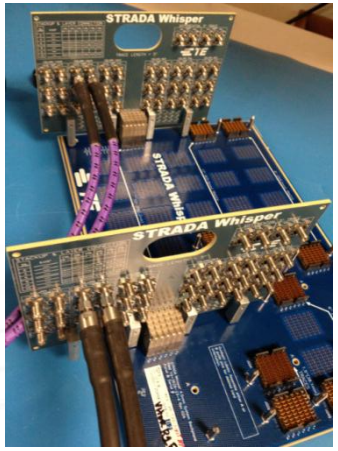
Will repeat demo at OFC

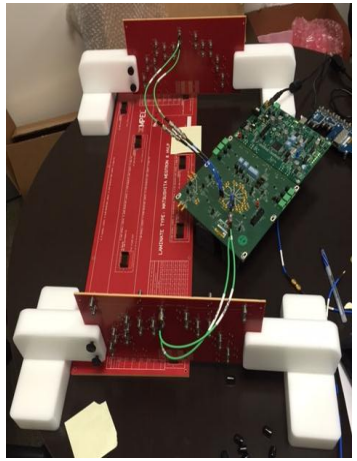
- **50G PAM4**
  - 50G PAM4 demo: error-free operation on **40in Molex Impel Meg6 Backplane** designed for 100GBASE-KR4
  - 50G PAM4 demo: error-free operation on **40in TE Backplane** designed for 100GBASE-KR4
  - 30~31dB insertion loss (not including test cables), crosstalk, Pre-FEC BER ~= 1e-10
  - No external intervention – equalization, adaptation, FEC, are all on-chip

40G PAM4 TE connectivity



TE connectivity **50G PAM4** molex





MEASURED POWER

- **Multiple test chips demonstrates accurate correlation between actual chip power consumption and design target power (even over process, voltage and temperature)**
  - Validates accurate extraction and power estimation, excellent library models/characterization
  - Excellent correlation (SNR/BER) between simulation results and actual silicon performance

- **Measured power extrapolated to 16nm (including FEC/sync. state machines etc.)**

LR	< 350mW	6.3 pJ/bit
MR	< 200mW	3.6 pJ/bit
VSR	< 150mW	2.7 pJ/bit

CONCLUSIONS

- **Single modulation serves multiple reaches**
- **Efficient IP design reuse (PLL, TX design can be reused to support multiple reaches)**
- **Natural progression to higher speeds**
  - Evolution is an integral part of technology advancement