Decoupling electrical and Optical Modulation

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- Rich Mellitz, Intel
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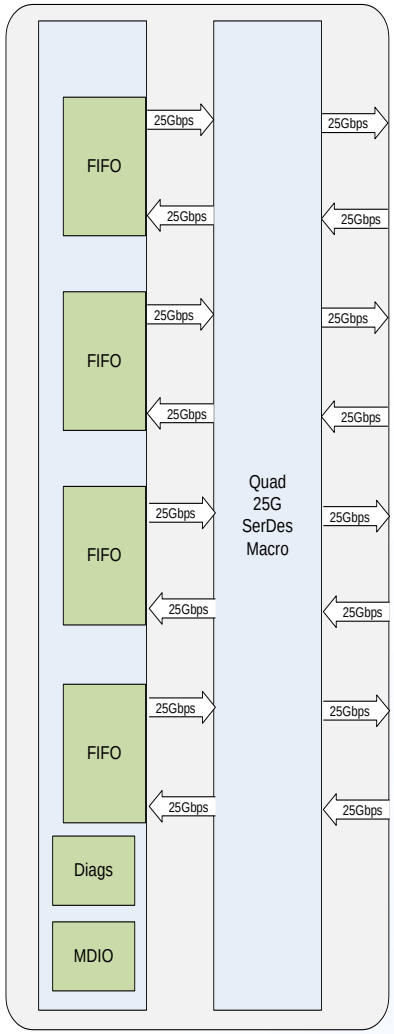
Overview

- There is a belief that there should be a linkage between the electrical modulation used on CDAUI-8 and Optical modulation used for SMF PHYs
  - This is based on the assertion that not changing modulation will "keep things simple" and lead to a lower power and area solution
- This presentation asserts that this belief is unfounded for CMOS re-timers

Recap of szczepanek_02_0312_NG100GOPTX

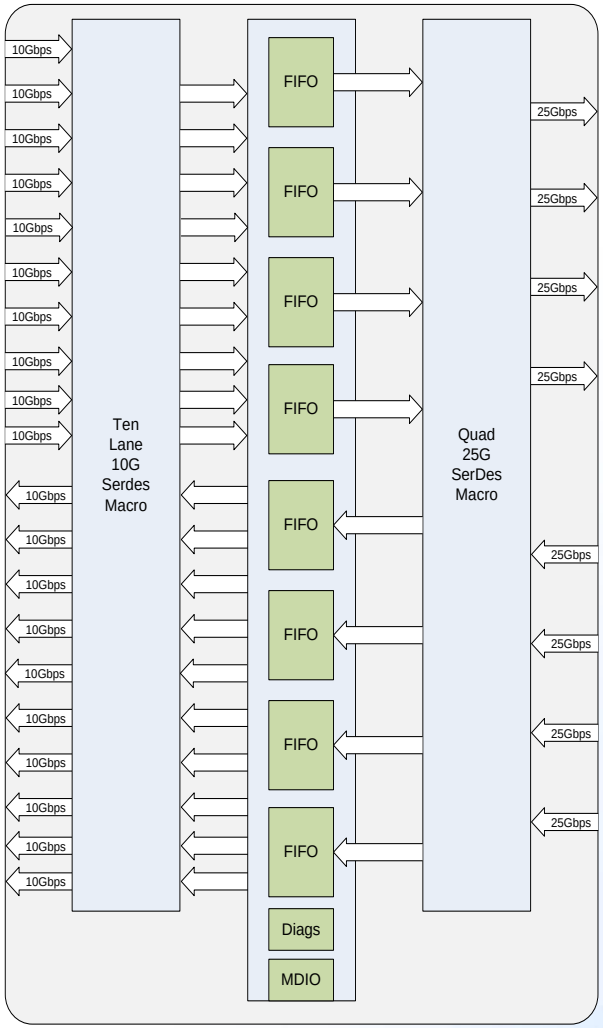
- CMOS architectures for 100G re-timers & Gearboxes based on re-usable SERDES macro building blocks are dominated by SERDES power and area

Slide 7, szczepanek_02_0312_NG100GOPTX.pdf : Implementation complexity of CMOS VSR re-timer



- CMOS retimers, can be based on a 28G Serdes macro + synthesized (skew) FIFOs
  - Power is dominated by Serdes macro, not FIFO function
  - Non-Serdes power is <5% of device power for Inphi retimer

Slide 8, szczepanek_02_0312_NG100GOPTX.pdf : Implementation complexity of CMOS VSR gearbox



- A CMOS 10:4 gearbox is also based on Serdes macros + synthesized (skew) FIFOs & VL muxing
  - Power is still dominated by Serdes macro, not FIFO functions
  - Non-Serdes power is <6% of device power for Inphi gearbox
  - Only 1% more power than for a CMOS re-timer

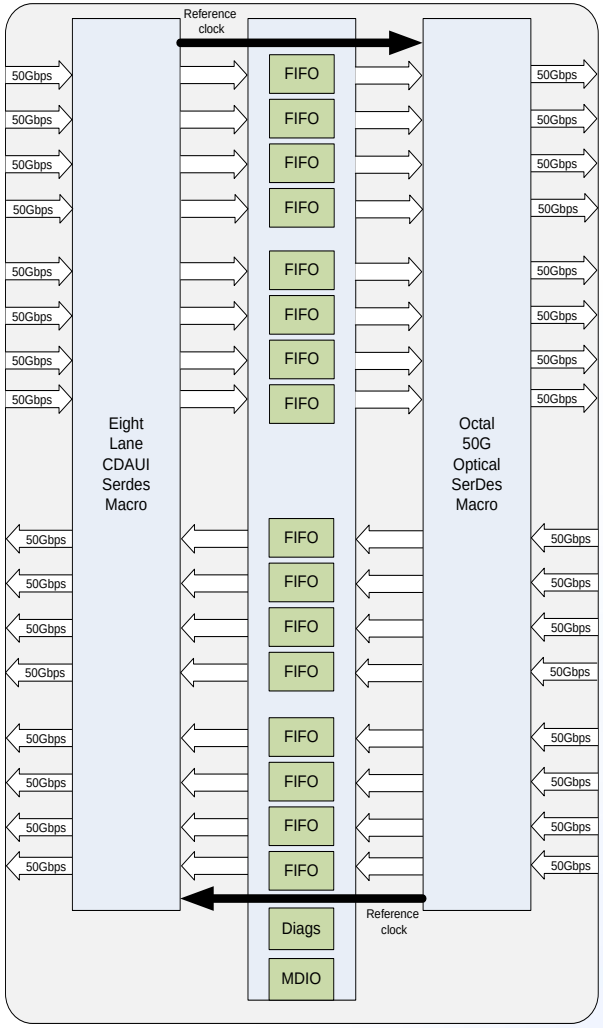
Clocking in a CMOS Serdes Macro

- In CMOS Serdes IP Receive and transmit functions are clocked separately
  - The Receiver “Clock and Data Recovery” function produces multi-phase clocks for parallel data samplers
    - sampling at 25GHz is not practical in CMOS
    - Rx CDR is based on a common PLL plus phase interpolators or per lane PLLs
  - A Transmit PLL produces multi-phase clocks for interleaved data drivers (driving at 25Gbd is again not practical in CMOS)
    - The Tx PLL uses a reference clock from the receiver, this clock is a relatively slow clock (say 644MHz)
    - An LC Tx PLL can be used to reduce jitter transfer
- The FIFO between Receive and Transmit removes instantaneous phase variations between Rx and Tx PLLs
- As long as Receive and Transmit baud rates are harmonically linked, modulation type doesn’t matter

Relevance to 400G re-timers and Modulation

- CMOS Re-timers for 400G will be built like 100G re-timers
  - Built from re-useable Serdes IP building blocks.
    - Which will also be used in other products, or sold as IP
- Therefore CDAUI and Optical Serdes are independent and can use different modulation schemes
- The complexity of the FIFO needed between the Serdes depends only on clock rate and bus width, NOT modulation.
  - The FIFO between an NRZ Serdes and a PAM4 Serdes is no more complex than that needed between NRZ & NRZ, or PAM4 & PAM4 (based on same bus width)
- So I estimate the non-Serdes functions to again be <5% of Serdes power for a 400G re-timer

Implementation complexity of 400G CMOS re-timer



- A CMOS 400G re-timer can also be based on Serdes macros + synthesized (skew) FIFOs
  - Although Octal Macros are shown, Single, dual or Quad macros may also be used.
  - Power and area are dominated by the Serdes macros, not FIFO functions
  - Non-Serdes power is <5% of device power based on 100G experience

Conclusions

- For CMOS implementations there is no Power/Area advantage in coupling Electrical and Optical modulation
  - There is obviously less development effort if the same IP can be used for both interfaces
- There will be a clear Power/Area disadvantage if either Interface has to operate with two different modulation schemes at the same data-rate