

OTN Support Proposal

P802.3bs 400 Gb/s Ethernet Task Force

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Supporters

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OTN Mapping Reference Point Baseline Adopted January 2015

Motion 5: Move to adopt slide 10 of [trowbridge 3bs 01a 0115.pdf](#) as the baseline for the OTN mapping reference point

M: Steve Trowbridge

S: Pete Anslow

Technical $\geq 75\%$

Y: 74; N: 0; A: 43

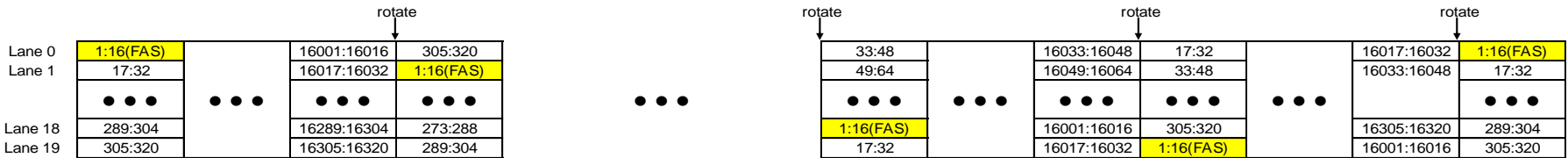
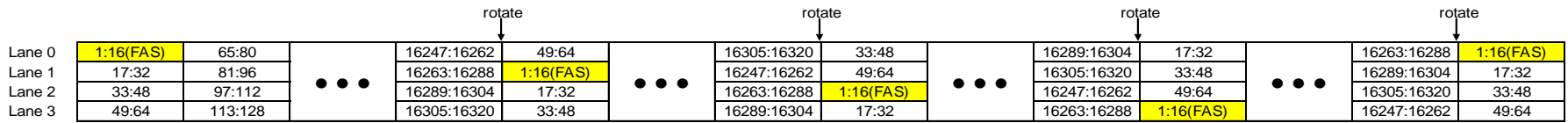
Motion passes

Remaining OTN Support

“Big Ticket Item” – Module Reuse

- Classic OTL approach:
 - If all current and future 400GbE PMDs use the same logical lane architecture (e.g., striped into the same number of PCS lanes) and if the PMA multiplexing is bit-pattern agnostic (e.g., bit multiplexing), then the only constraint is to be able to stripe the OTN frame into the same number of PCS lanes as Ethernet
- Stripe OTN frame as Ethernet approach:
 - If some current or future 400GbE PMDs might use a different logical lane striping, or if PMA multiplexing is not bit-pattern agnostic (e.g., 10-bit RS symbol multiplexing anchored to Ethernet lane alignment markers), it may be necessary to make the OTN frame look enough like Ethernet to get it through the module.

Classical OTL striping for OTU3 and OTU4



- Stripe OTU3 or OTU4 frame in 16-byte increments
- Rotate lane assignments at each frame boundary so that each lane sees an OTN framing pattern once per 4080×4 bytes
- OTU3 uses two lower order bits of MFAS as a lane marker
- OTU4 “borrows” 3rd OA2 byte as a lane marker
- Similar method can be used for striping into 16, 8 or 4 logical lanes since $n \times 4080 \times 4$ bytes is divisible by 16, 8 or 4

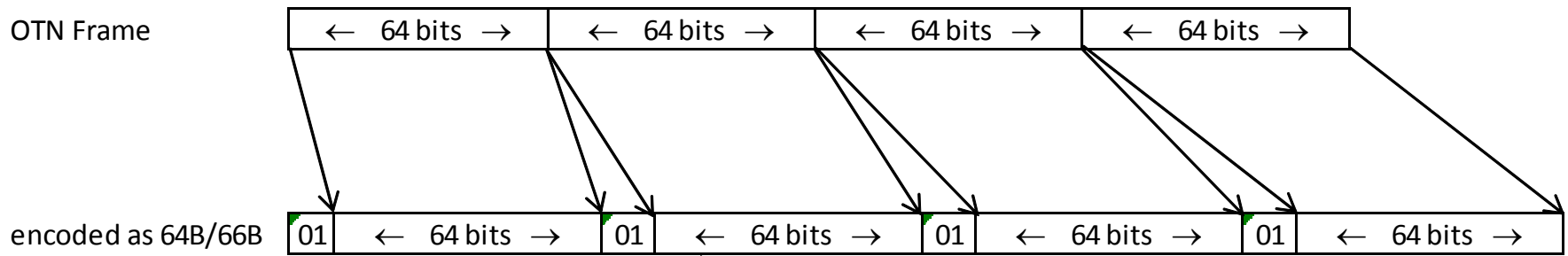
Striping OTN frame as Ethernet option

- Use the fact that the OTN mapping reference point, is a logically serial stream of 64B/66B blocks.
- Note that before this reference stream can be physically instantiated, it must be striped over multiple physical or logical lanes
- Maintain the principle, as in 802.3ba, that idle insertion/deletion is not done below this reference point.

Implications for OTN

- Likely only possible if the same FEC code can be used for OTN applications as for Ethernet applications at about 6% higher bit-rate
- Would need to make OTN look like 66B blocks. Easiest way to do this and not lose any information in transcoding is to insert a “01” sync header after every 64 bits (all data)
- Since this is just part of the logical frame format, this doesn't waste as many bits as it appears. 8 sync header bits are added to every 256 data bits in the “logical” frame format, but 7 of those bits are immediately recovered in 256B/257B transcoding and reused for the FEC code. So 0.39% net is added to the OTN frame to make it look like 66B blocks, RS FEC added

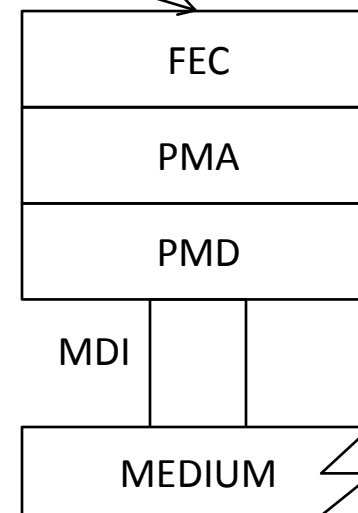
Illustration of turning OTN frame into 64B/66B blocks



Use the Ethernet Stack to stripe and FEC encode the OTN frame when carrying over an Ethernet Module for an OTN IrDI or client interface

Could be OTN frame aligned as an OTUC4 frame without FEC is exactly 7648×64 bits, but not essential with scrambling

Scramble



OTN Bit-rates using this scheme

Updated assuming KP4 FEC

	Working Assumption Bit-Rate
OTUC4 bit-rate without FEC	422.904 Gb/s
64B/66B encoded	436.120 Gb/s
256B/257B transcoded	424.556 Gb/s
Insert Lane Markers	424.582 Gb/s
Add RS(544,514) FEC	449.363 Gb/s
Logical Lane Rate (within CEI-28G)	28.085 Gb/s
Ethernet Nominal Bit-rate	425 Gb/s
400G OTN Increase in bit-rate	5.73 %
100G OTN Increase in bit-rate	8.42 %

Smaller increase for 400G than for 100G, mainly due to using same percentage overhead FEC

Recommended module reuse mechanism for OTN

- There is an Ethernet sublayer reference point that can accept a serial stream of 64B/66B blocks (the same as the adopted OTN mapping reference point)
- No idle insertion/deletion occurs below that reference point, and hence the rest of the stack can deal with a constant-bit-rate (CBR) bitstream that is effectively an infinite-length packet.
- Note that any logical to physical lane interleaving that works for Ethernet also works for OTN since they are encoded the same way
- The link parameters and FEC coding gain have sufficient margin to meet the error performance target when running at approximately 5.73% higher bit-rate than necessary for 400G Ethernet

THANKS!