IEEE P802.3bs 400 Gb/s Ethernet Task Force
Informal Communication

Source:	IEEE P802.3bs 400 Gb/s Ethernet Task Force[1]	
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Subject:	Informal communication to OIF on progress in IEEE P802.3bs 400 Gb/s Ethernet Task Force	
Approval:	Agreed to at IEEE P802.3bs 400 Gb/s Ethernet Task Force meeting, Berlin, Germany, 12 March 2015	

Dear Mr. Tracy and members of OIF,

As you may know, the P802.3bs Task Force is still in the process of choosing baseline proposals to address all of the project objectives. We would like to inform you of additional baseline proposals adopted during our March 2015 meeting in Berlin, Germany.

The baseline proposals adopted so far in the P802.3bs project include the following:

Baseline adopted in San Diego meeting (July 2014):

- adopt the baseline for the CDMII logical interface as shown in slide 5 of gustlin_3bs_03_0714.pdf

Baselines adopted in Kanata, Canada meeting (September 2014):

- adopt 16 x 25Gb/s and 8 x 50Gb/s as the basis for the lane rates for any optional C2C and C2M electrical interfaces
- adopt the P802.3bm C2C and C2M specifications with current values (except that the BER requirement is TBD) as a baseline draft for the 16 x 25Gb/s electrical interfaces

[1] This document solely represents the views of the IEEE P802.3bs 400 Gb/s Ethernet Task Force, and does not necessarily represent a position of the IEEE, the IEEE Standards Association, IEEE 802 or the IEEE 802.3 Working Group

Baselines adopted in San Antonio, TX meeting (November, 2014):

- adopt the proposal in slides 6 to 16 in king_3bs_02a_1114.pdf as the baseline proposal for the P802.3bs objective to “provide physical layer specifications which support link distances of at least 100 m of MMF” (400GBASE-SR16)

Baselines adopted in Atlanta, GA meeting (January 2015):

- adopt slides 4 and 8 from dambrosia_02b_0115.pdf as baseline architecture
- adopt the EEE baseline proposed in marris_3bs_01_0115.pdf slide 7
- adopt slide 10 of trowbridge_3bs_01a_0115.pdf as the baseline for the OTN mapping reference point
- adopt the following equation as the informative insertion loss equation for CDAU-8 chip-to-chip electrical I/O interface: IL≤{1.083+2.543 SQROOT(f)+0.761f 0.01≤f≤28.05GHz} dB
- adopt the following equation as the informative insertion loss equation for CDAUI-8 chip-to-module electrical I/O interface: IL≤{1.076(0.075+0.537SQROOT(f)+0.566f) 0.01≤f≤28.05GHz} dB

Baselines adopted in Berlin, Germany meeting (March 2015):

- adopt RS(544,514,10) as the FEC in the 802.3bs 400GbE architecture (note, however, that it has not been decided whether this FEC will be organized on a 4x100G or 1x400G basis)
- adopt li_3bs_01a_031.pdf as the baseline proposal for CDAUI-8 chip-to-chip electrical I/O interface except for the differential return losses (on slide 11) for the Tx and the Rx shall be TBD
- adopt brown_3bs_01a_0315.pdf as the baseline proposal for CDAUI-8 chip-to-module electrical I/O interface

Action items have been identified to be worked prior to the next meeting with a view toward being able to adopt remaining logic (e.g., PCS, PMA) and optical interface baselines.

Information from our most recent meeting is available at:

http://ieee802.org/3/bs/public/15_03/index.shtml

Sincerely,

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