Further Investigation of Bit Multiplexing in 400GbE PMA

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Introduction and Background

- Bit-Mux in PMA is a general advantageous for simple optical module implementation to lower cost, power and form factor
- This presentation investigates the Bit-Mux in PMA and its influence to FEC performance on different error model and multiplexing scheme

Big Ticket Items - PMA

- PMA reference presentations:
  - Slavick_3bs_01_0115.pdf
  - Wang_t_3bs_01_0115.pdf
  - Gustlin_3bs_02_0115.pdf
- Actions:
  - PMD selection and electrical interfaces will impact Muxing scheme

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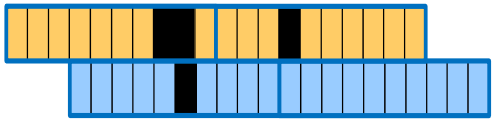
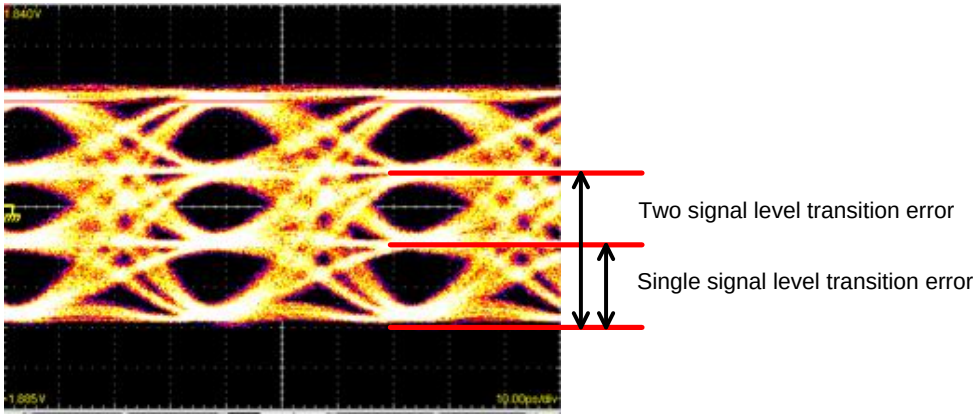
Error Models in PAM4 Signaling

- Random errors introduced by Additive White Gaussian Noise (AWGN)
  - Consecutive and discrete random error bits on PAM4 2:1 bit muxing



  - Consecutive and discrete random error bits on PAM4 4:1 bit muxing

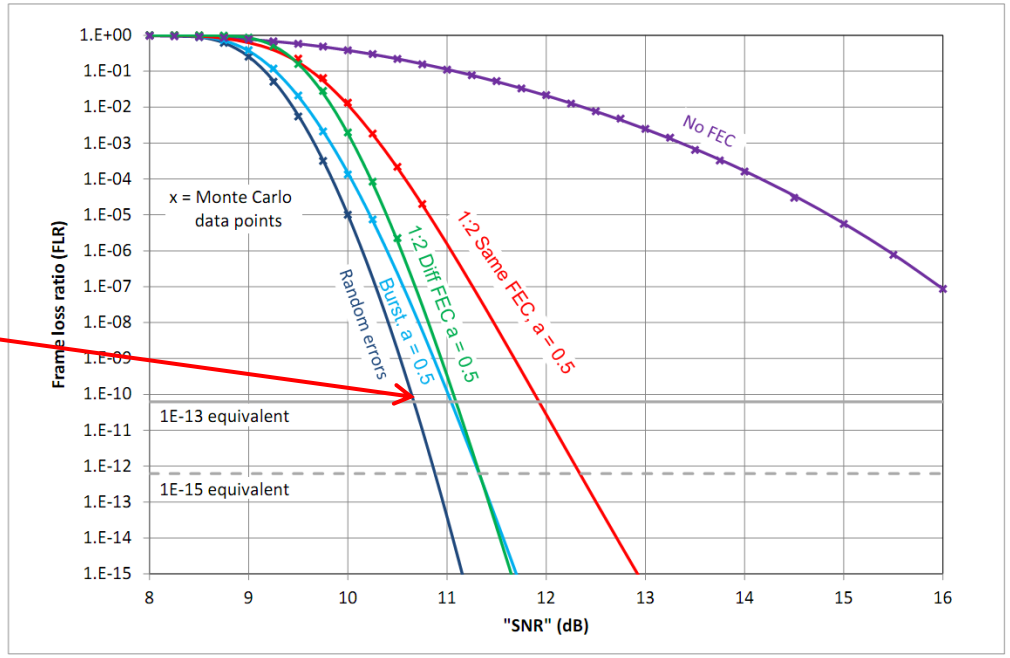
- Crosstalk or interference noise are different to AWGN, it leads to consecutive or discrete error, possibly overlays on random error by AWGN noise.
- Correlated error induced by electronic equalizer, for example DFE or MLSE, is possible of having single or two signal level transition errors.



FEC Performance on PAM4 Bit-mux with Random Error by AWGN

- Random error model for any error patterns, including burst error by Additive White Gaussian Noise (AWGN), is depicted in the “light dark” curve.
- Crosstalk, interference error should be covered by system design, also depend on FEC margin to cover these consecutive/discrete bit errors.

- FEC performance of random error caused by AWGN, not including crosstalk or interference errors.



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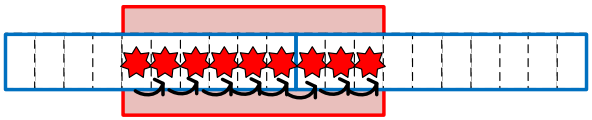
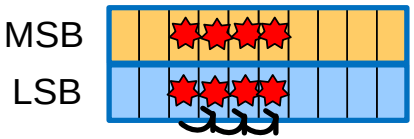
FEC Performance on PAM4 bit-mux with Error Propagation

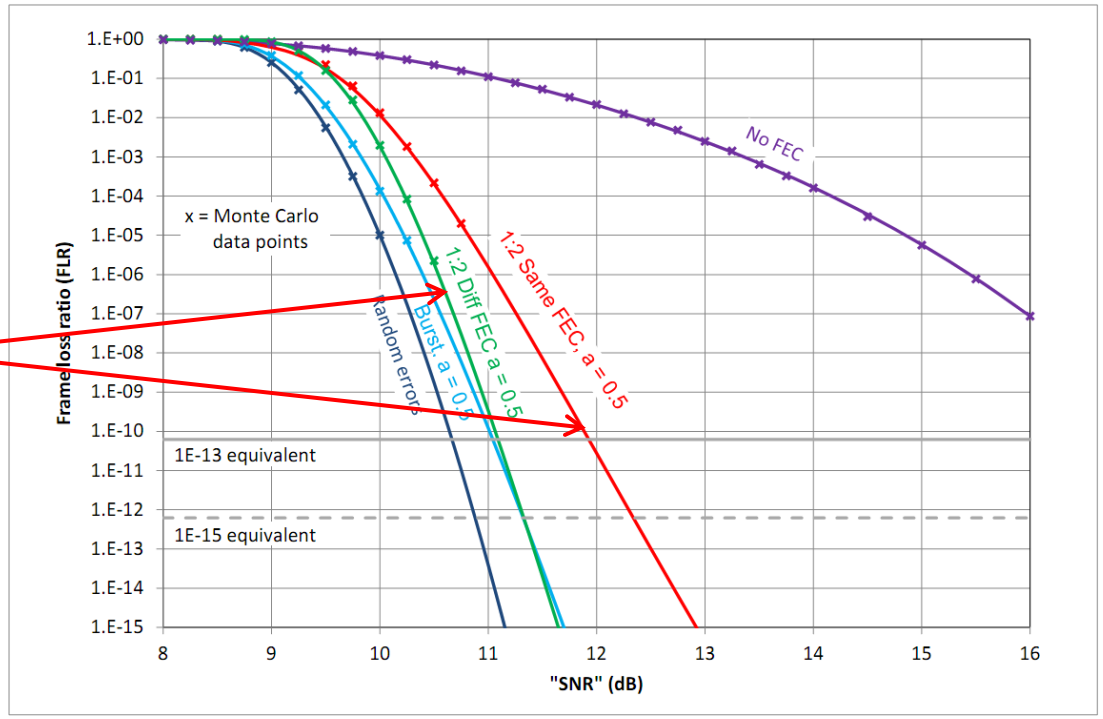
- Correlated error induced by electronic equalizer, will lower FEC performance in Non-FOM bit muxing. Two signal level transition error that corrupt both MSB/LSB in PAM4 has similar FEC performance as NRZ signaling

Correlated error caused by error propagation on NRZ



Correlated error caused by error propagation on PAM4





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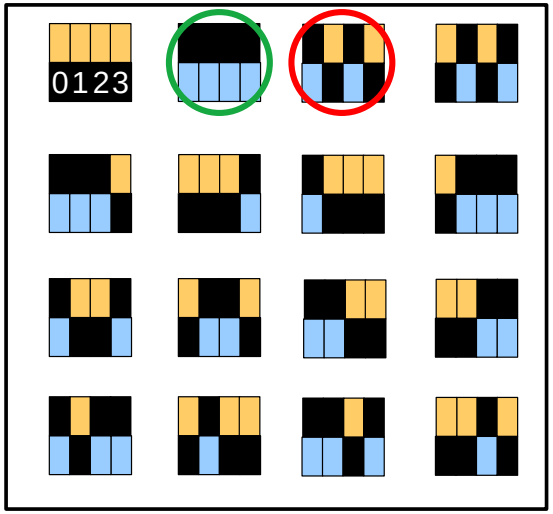
FEC Performance on PAM4 bit-mux with Error Propagation (Cont'd)

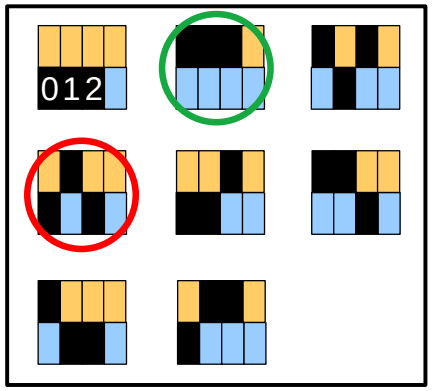
- PAM4 correlated error performance?
  - Two signal level transition has worst FEC performance
  - Single signal level transition error incurs only a single bit error per PAM4 symbol with gray coding, happens on either MSB or LSB
- Considering different error patterns in 4 PAM4 symbol with correlated errors with single signal level transition error , what is the impact on FEC performance with FOM bit muxing and Non FOM bit muxing?
  - Correlated error longer than 4 symbol has lower probability
  - Any error patterns in 4 PAM4 symbol are possible, use worst case error pattern to evaluate FEC performance in this contribution

PAM4 Error Patterns for Single Signal Level Transition Error

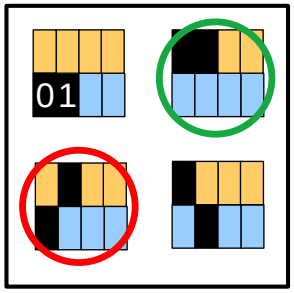
- 4/3/2 PAM4 symbol correlated error have following error patterns:



Error patterns in 4 symbol burst error

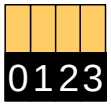


Error patterns in 3 symbol burst error



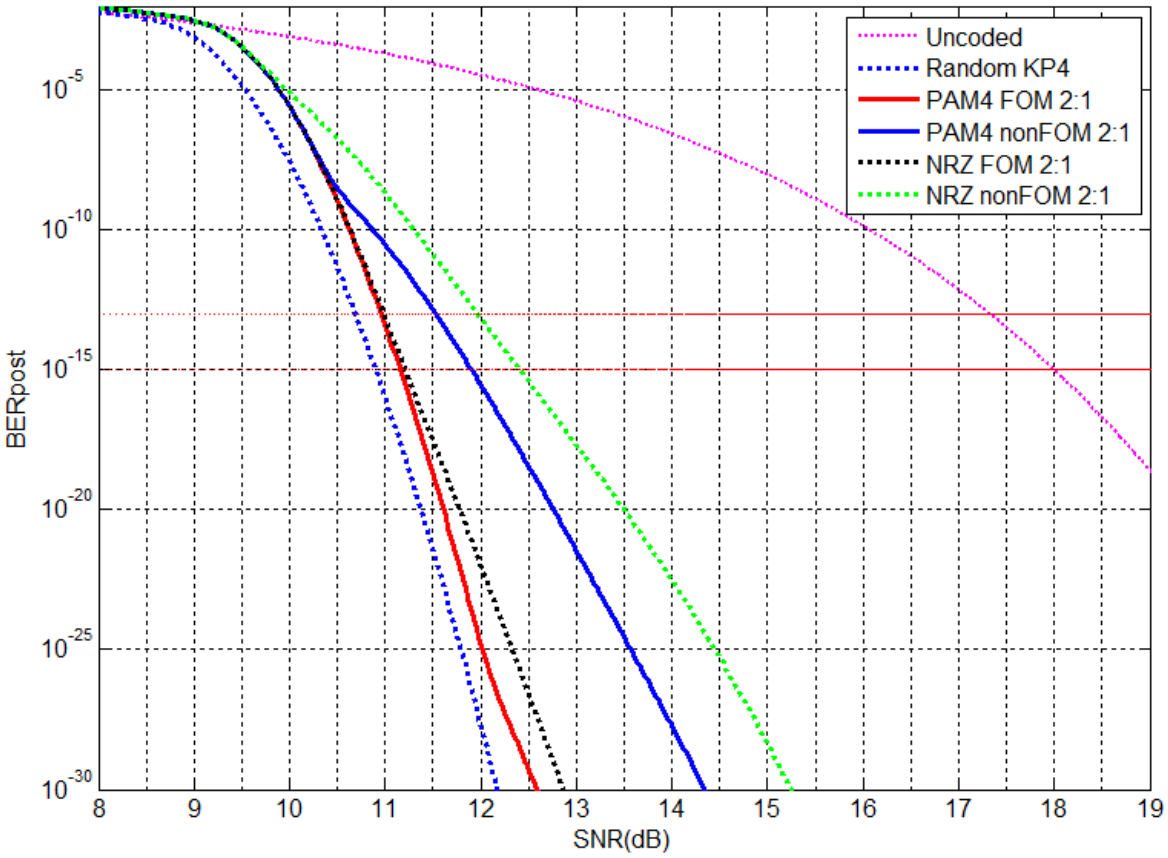
Error patterns in 2 symbol burst error

- Each error pattern has different impact on FEC Performance



  - For example, the left error pattern will cause 1 symbol error by 35% and 15% 2 symbol error in FOM bit mux
  - Red circle in diagram indicates the worst case for FOM bit muxing, green circle for nonFOM bit muxing

KP4 FEC Performance on PAM4 bit-mux with Single Signal Level Transition Error



- Assume error propagate parameter a=0.5
- With KP4 FEC, FOM bit muxing performance is close to random error curve on PAM4 and NRZ
- Non FOM bit muxing will degrade FEC performance

DFE in Electrical Link

- For CDAUI-16 specification in 802.3bs, reference to Chip-Chip interface of CAUI-4 in 802.3bm

Introduction

If a DFE is assumed to be part of the receiver for CAUI-4 chip-to-chip (C2C), then the probability of burst errors is much greater than for receivers that do not employ DFE. The likely presence of burst errors would call in to question the mean time to false packet acceptance (MTTFPA) performance of a link using CAUI-4.

Because of this, the reference receiver assumed for CAUI-4 C2C in P802.3bm D1.1 employs a CTLE but no DFE.

However, there has been discussion within the P802.3bm Task Force and the CAUI-4 Ad Hoc suggesting that the restriction in performance due to assuming a CTLE only reference receiver severely restricts the broad market potential of the CAUI-4 C2C solution.

This presentation attempts to analyse the impact of a DFE in the CAUI-4 C2C receiver on the MTTFPA performance.

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- For Chip-Chip PAM4 proposal of CAUI-8 interface in 802.3bs

Technology Choice Highlights 1

- Channel target/requirement based on that of "informative insertion loss budget" from the electrical interface ad hoc
  - PAM-4 signaling and system is intended to work over existing CAUI-4 c2m and c2c infrastructures
- Channel equalization based on a transceiver having TX FIR, RX CTLE and DFE

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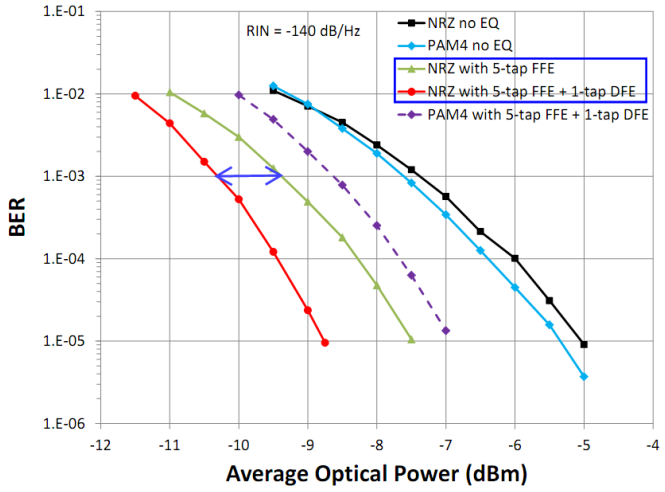
DFE Usage in NRZ Optical Link

- For example, ~1dB gain from DFE to improve RX optical sensitivity as in light blue measure

- With a=0.5, The penalty of DFE is only ~0.3dB for KP4 FEC with FOM bit mux

56 Gb/s Monte-Carlo Simulation Results



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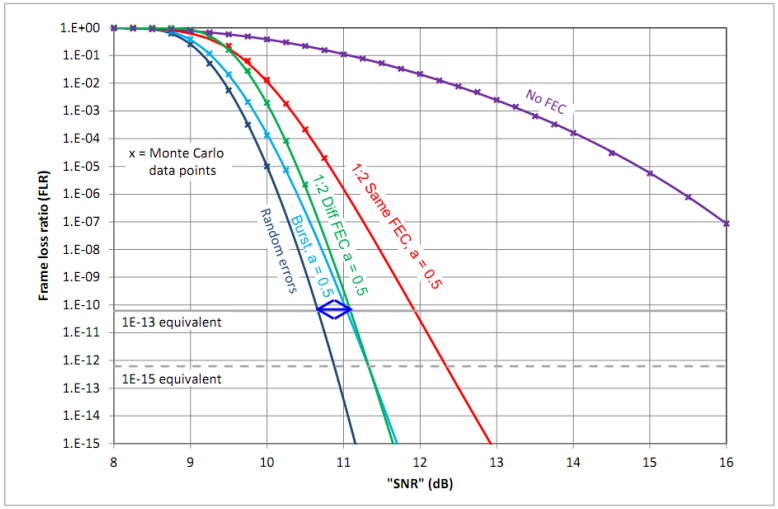
RS(544,514) all curves



- With FOM bit-mux, KP4 FEC performance will be close to random error curve with error propagation by DFE in RX Equalizer,

DFE/MLSE Usage in PAM4 Optical link

- Chris Cole, Ilya Lyubomirsky, Ali Ghiasi, Vivek Telang, “Higher-Order Modulation for Client Optics”, IEEE Communications Magazine, March 2013
  - Figure 2 shows an RX DSP-based adaptive equalizer with feed-forward equalizer (FFE) and decision feedback equalizer (DFE) blocks.
  - An FFE is characterized by the number of taps and their spacing; either T-spaced (symbol rate) or T/2-spaced (fractional). An FFE approximates the channel matched filter response and equalizes the precursor portion of the ISI.
  - A DFE is characterized by the number of taps and cancels the post-cursor portion of the ISI.

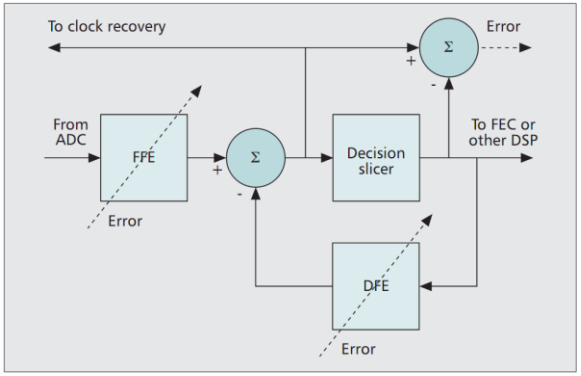
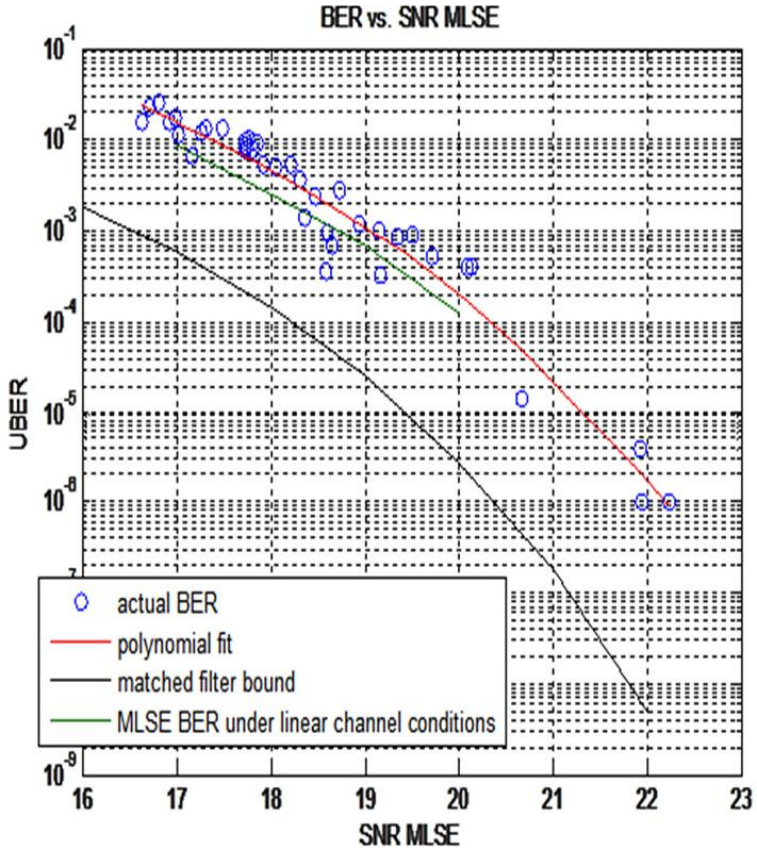


Figure 2. *RX DSP adaptive equalizer block diagram.*

- “PAM-4 Four Wavelength 400Gb/s solution on Duplex SMF” in conroy_3bs_01a_0914



BER Requirement of Electrical Link with Non-FOM Bit Mux

- According to previous FEC performance evaluations (anslow_3bs_02_1114),

			RS(528,514)		RS(544,514)		BCH(2858,2570) t=24	
	Electrical	Optical	FLR = 6.2E-11	FLR = 6.2E-13	FLR = 6.2E-11	FLR = 6.2E-13	FLR = 6.2E-11	FLR = 6.2E-13
1:2 Same FEC, a = 0.5	Burst	Random	4.6E-8*	5.4E-9*	7.5E-6*	3.4E-6*	6.6E-9*	1.4E-10*
	Burst	Burst	7.5E-8*	8.4E-9*	1.4E-5*	7.1E-6*	1.4E-7*	1.7E-9*
Single FEC burst, a = 0.5	Burst	Random	2.9E-6*	1.0E-6*	4.4E-5*	2.9E-5*	6.6E-9*	1.4E-10*
	Burst	Burst	3.6E-6*	1.3E-6*	5.1E-5*	3.4E-5*	1.4E-7*	1.7E-9*
1:2 Different FEC, a = 0.5	Burst	Random	3.9E-6*	1.6E-6*	4.2E-5*	3.0E-5*	1.7E-5*	3.1E-6*
	Burst	Burst	4.6E-6*	2.0E-6*	4.7E-5*	3.4E-5*	5.5E-5*	2.6E-5*
Random errors	Random	Random	1.2E-5	7.2E-6	8.2E-5	6.2E-5	3.3E-4	2.8E-4

- Non-FOM bit mux proposal with KR4 FEC will require 4.6E-8 BER in multiple part link, including electrical and optical links;
  - Or to shorten channel length to lower Insert loss or improve target BER of CDAUI-8
- If use KP4 FEC for all PMDs in 802.3bs, it will require MMF PMD operating at 3% Over-clocking.

Comparison of FOM/NonFOM Bit-Mux

	Pros	Cons
Non-FOM Bit mux	One FEC instances Architecture	Degraded FEC performance in face of error propagation
	No additional electrical interface layout rule	Almost rule out DFE/MLSE like electrical equalizer in Optical link
		If KR4 FEC in host, electrical interface will operate at ~1E-8 or limited to short channel
		If only KP4 FEC in host to match 1E-6 BER target in electrical interface, mmf PMD will operate at 3% over-clock
		Not robust to burst error introduced by interference on optical link
		Not robust to burst error introduced by crosstalk on multi-lanes electrical interface
FOM Bit Mux	Close to Random error FEC performance in face of error propagation	Multi-FEC instances Architecture
	Enable DFE/MLSE like equalizer in Electrical/Optical link	Additional electrical interface layout rule required
	Match 1E-6 BER target in C-C/C-M CDAUI-8 interface	
	No requirement of 3% over-clock if MMF PMDs reuse 802.3bm specification	
	Robust to burst error introduced by interference/crosstalk	

Summary

- PMA Option 1:

  Prefer to use FOM bit multiplexing as primary scheme for a robust logic architecture

- PMA Option 2:

  Use NON-FOM bit multiplexing if all the listed implementation constrains are satisfied

Thank you