Chief Editor’s report

Pete Anslow, Ciena, P802.3bs Chief Editor

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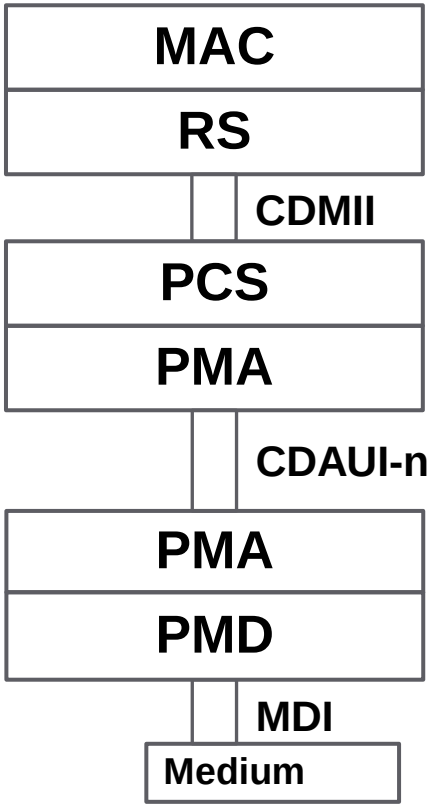
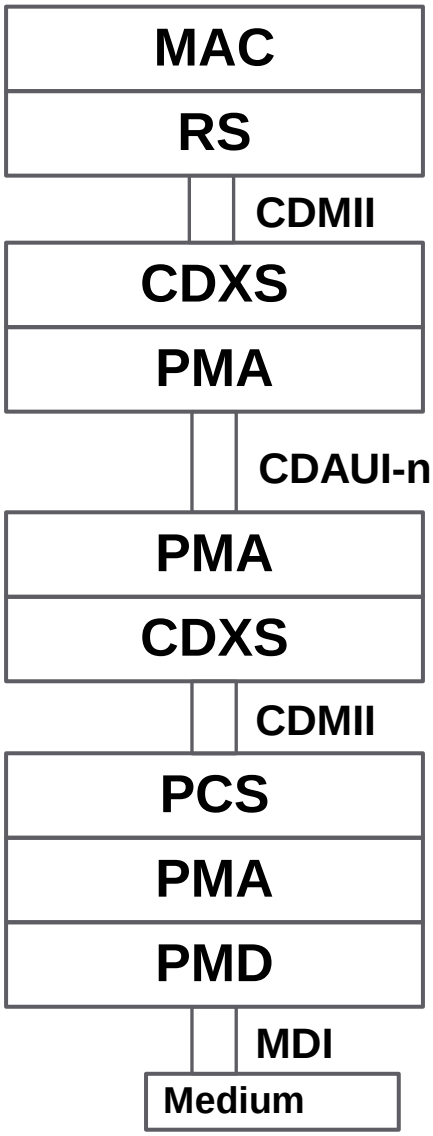
Introduction

The following slides contain:

- the proposed structure for the P802.3bs 400 Gb/s Ethernet draft amendment
- list of editors for adopted baselines
- a list of open questions for adopted baselines

Adopted stack





When PCS functions and CDXS functions do not match

New clauses

Clause	Content	Baseline
116	Introduction to 400 Gb/s networks	
117	RS and MII for 400 Gb/s operation	
118	CDMII extender (includes CDXS)	Baseline adopted
119	PCS including FEC	Need baseline
120	PMA	Need baseline
121	400GBASE-SR16	Baseline adopted
122	PMD clause for 500 m objective	Need baseline
123	PMD clause for 2 km objective	Need baseline
124	PMD clause for 10 km objective	Need baseline
120A	Partitioning examples (informative)	
120B	CDAUI-16 chip-to-chip (normative)	Baseline adopted
120C	CDAUI-16 chip-to-module (normative)	Baseline adopted
120D	CDAUI-8 chip-to-chip (normative)	Baseline adopted
120E	CDAUI-8 chip-to-module (normative)	Baseline adopted

Amended clauses

Clause	Change	
1	Add new references, definitions, abbreviations	
4	Add 400G parameters to Table 4-2	
30	Add new management objects / attributes	
45	Add new registers / bits	
78	Add new EEE PHYs	Baseline adopted
Annex A	Add any new bibliography entries	
Annex 4A	Add / modify note to Table 4A-2	
Annex 31B	Add 400G PAUSE information	

Editorial team (for adopted baselines)

Pete Anslow, Ciena

- Chief Editor and Editor for Clauses 00, 1, 4, 30, 45, 78, A, 4A, 31B, 116, 118

Mark Gustlin, Xilinx

- Editor for Clauses 117

Jonathan King, Finisar

- Editor for Clause 121

Andre Szczepanek, Inphi

- Editor for Annexs 120D, 120E

Open questions for CDAUI-16 chip-to-chip

- BER requirement is TBD
- Adoption of RS(544,514,10) FEC increases the signalling rate from 25.78125 GBd for CAUI-4 to 26.5625 GBd. What changes are needed to the specification to account for this?
- The optional transmitter equalization feedback for CAUI-4 chip-to-chip can use MDIO registers 1.180 to 1.187 (8 registers). Should CDAUI-16 define 32 new registers for this purpose or 24 new and re-use the 8 existing CAUI-4 registers?

  Propose to define 32 new registers for this purpose. Any objections? Ok for CDAUI-8 to use 16 of these registers?

Open questions for CDAUI-16 chip-to-module

- BER requirement is TBD
- Adoption of RS(544,514,10) FEC increases the signalling rate from 25.78125 GBd for CAUI-4 to 26.5625 GBd. What changes are needed to the specification to account for this?
- CDAUI-16 will need a 16 way connector instead of a 4 way connector. Are there any changes required to the specification to account for this?
- Annex 83E for CAUI-4 chip-to-module requires that the host provides a “recommended CTLE peaking value”. There was some discussion before the baseline was adopted as to whether this would also be required for CDAUI-16.

Open questions for 400GBASE-SR16

- BER requirement given RS(544,514,10) FEC and sharing of the BER budget with electrical interfaces.
- Adoption of RS(544,514,10) FEC increases the signalling rate from 25.78125 GBd for 100GBASE-SR4 to 26.5625 GBd. What changes are needed to the specification to account for this?

Thanks!