400Gb/s 2km & 10km duplex SMF PAM-4 PMD Analysis & Measurements

400 Gb/s Ethernet Task Force

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IEEE

FINISAR

Introduction

- This presentation is in support of baseline proposal:

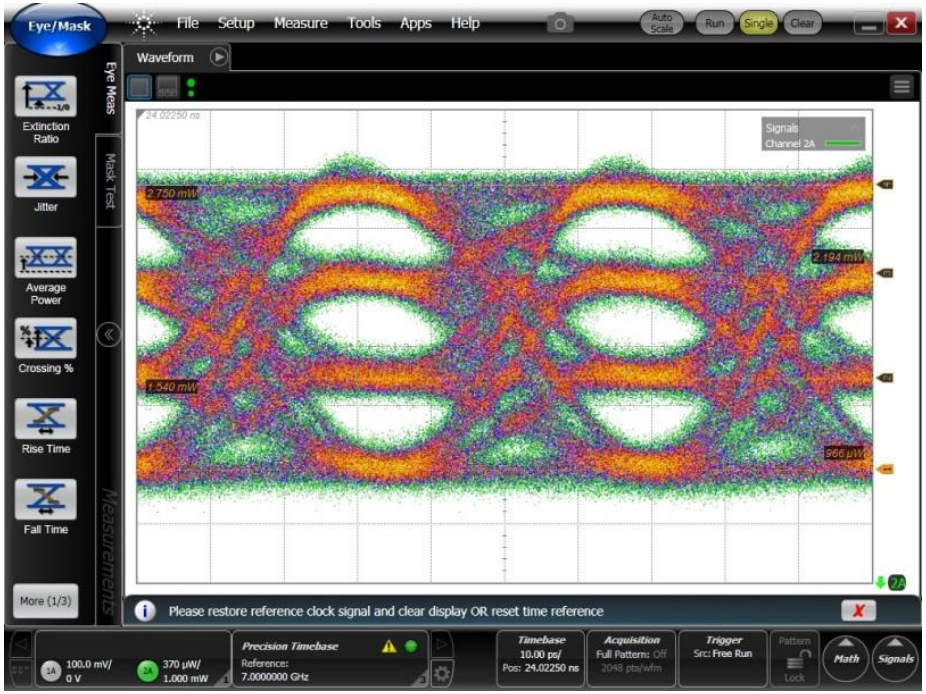
  400Gb/s 2km & 10km duplex SMF PAM-4 PMD Baseline Specifications, Cole et al. (cole_3bs_01_0515)

- BTIs:

http://www.ieee802.org/3/bs/public/15_01/big_ticket_items_3bs_01_0115.pdf#page=13

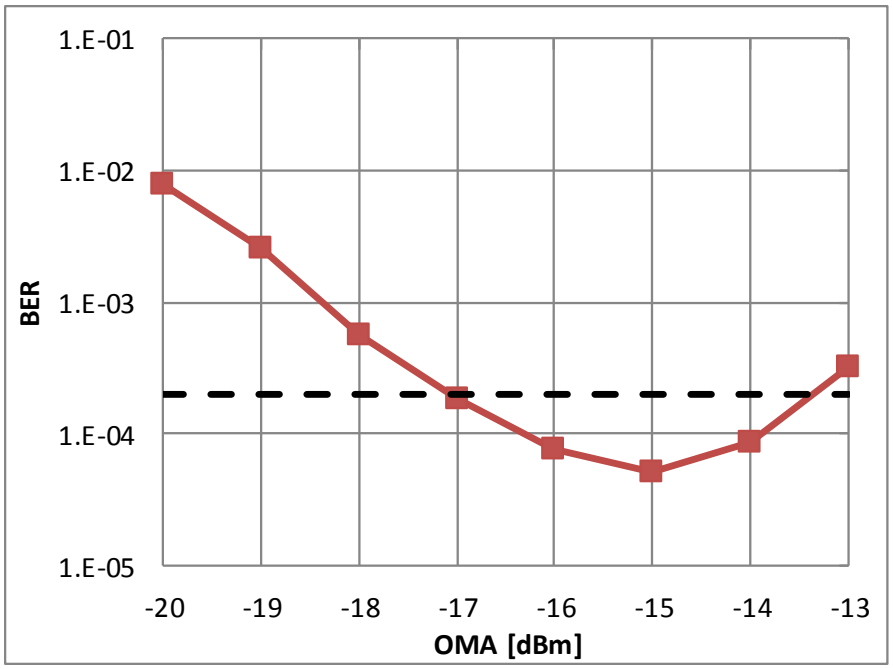
http://www.ieee802.org/3/bs/public/15_01/big_ticket_items_3bs_01_0115.pdf#page=19

Finisar PAM-4 BH-DFB DML TX Data



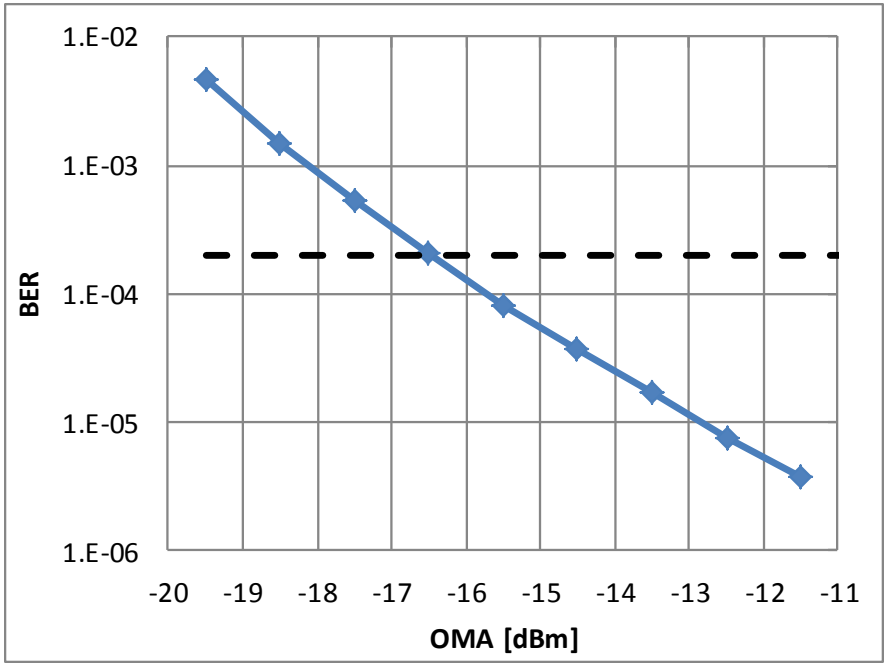
- Optical DCA eye
- 56Gb/s (28GBaud)
- SSPR
- 50^{o}C
- ER (11/00) = 4.7dB
- 60mA I_{bias}
- Finisar BH-DFB DML

Finisar PAM-4 BH-DFB DML RX Data



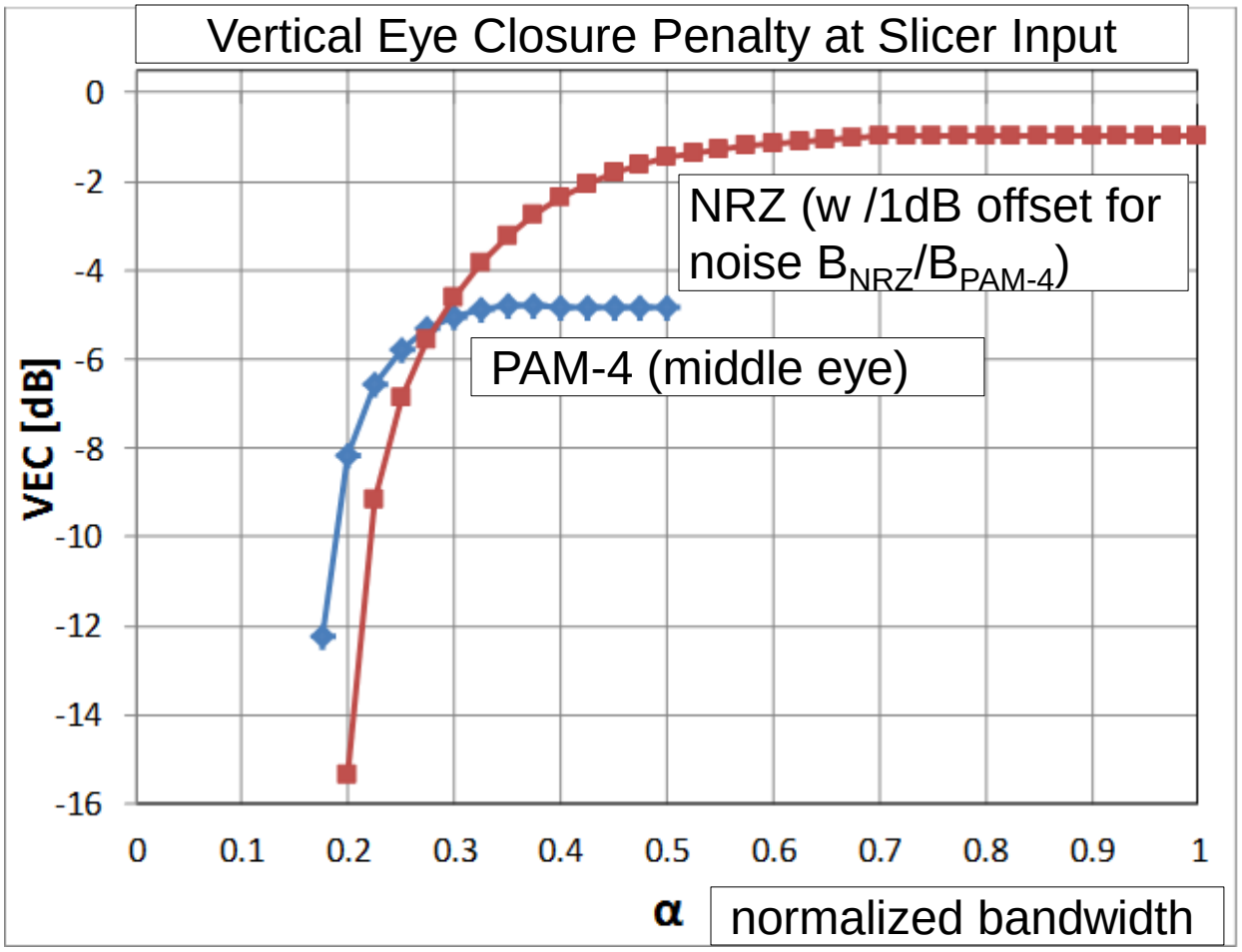
- 1309 λ BTB RX Sens. dBm OMA (inner eye)
- 56Gb/s (28GBaud)
- SSPR
- 5-tap T/2-spaced FFE
- BH DFB DML at 50°C
  - ER(11/00) = 4.7dB
  - 60mA I_{bias}
- PIN PD *R* = ~0.8A/W
- Limiting TIA
- TIA *N* = 16pA/√Hz
- TIA BW = ~27GHz
- TIA differential output

Finisar PAM-4 BH-DFB DML RX Data



- 1309 λ BTB RX Sens. dBm OMA (inner eye)
- 56Gb/s (28GBaud)
- SSPR
- 5-tap T/2-spaced FFE
- BH DFB DML at 50°C
  - ER(11/00) = 4.7dB
  - 60mA I_{bias}
- PIN PD *R* = ~0.8A/W
- Linear TIA
- TIA *N* = 12pA/√Hz
- TIA BW = ~20GHz
- TIA single-ended output

NRZ Adv.: SNR Penalty



cole_3bs_02_0315

PAM-4 permanently locks in SNR penalty which doesn't go away even as component bandwidth improves

NRZ Adv.: Development Risk

- NRZ is well understood
  - Specifications
  - Measurements
  - Development
  - Production
- PAM-4 requires a steep learning curve
  - Some lessons will be painful
  - Lots of humility is in order

PAM-4 Adv.: Optics Packaging & Reuse

- The baseline 8x50G PAM-4 2km and 10km PMD architecture enables reuse of high volume 100Gb/s Ethernet LR4 and CWDM4 QSFP28 OSA packaging:

  http://www.ieee802.org/3/bs/public/14_11/cole_3bs_02a_1114.pdf
- Analysis of 8x50G NRZ RF design indicates that improved OSA packaging and interconnect will be required, in particular new flex circuits for OSA to PCB 50G connections
- Alternately transceiver PHY IC will be required to be placed inside the OSAs

PAM-4 Adv.: 50G IC Availability & Ecosystem

- Most IC suppliers are developing 50G PAM-4 ICs
- Few PHY IC suppliers are considering developing 50G NRZ ICs
- Even if some PHY IC suppliers proceed with 50G NRZ IC development, this will dilute the supplier base effort

PAM-4 Adv.: 50G MMF PMD Compatibility

- PAM-4 advantages for 50G MMF PMDs
  - VCSEL availability
  - Lower penalties
- Common modulation format for SMF and MMF PMDs simplifies development and shares IC volume, similar to benefits between common modulation format for:
  - 10GBASE-SR & LR
  - 40GBASE-SR4 & LR4
  - 100GBASE-SR4 & LR4

Summary

Parameter	50G NRZ Advantage	50G PAM-4 Advantage
Optical SNR Penalty	X	
Development Risk	X	
Optics Packaging & Reuse		X
50G IC Availability & Ecosystem		X
50G MMF PMD Compatibility		X
Volume		X
Conclusion		X

400Gb/s PMD Analysis & Measurements

Thank you