Thoughts on the FEC Architecture

IEEE P802.3bs 400 Gb/s Ethernet Task Force

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1x400G vs. 4x100G FEC

- Seems like we have a PCS architecture that is agreeable to many (though it is not adopted yet)
- And an adopted FEC for that PCS architecture
- But we have not decided if we will have a single 1x400G FEC instance or 4x100G FEC instances
- This takes a look at some of the issues that have been brought up around this decision

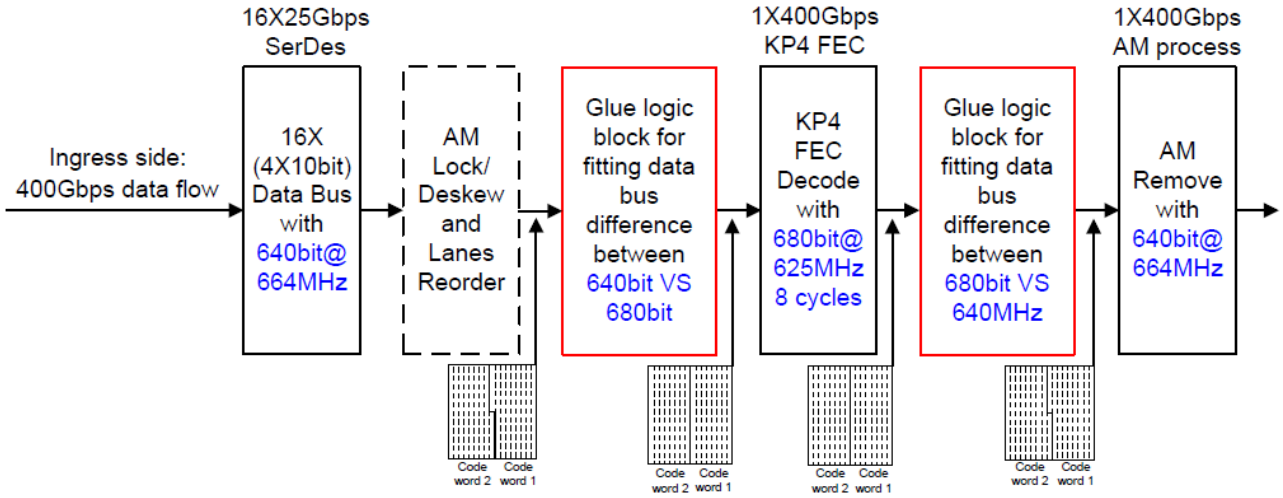
Breakout?

- If you care mostly about 4x100GbE breakout, then the 4x100G architecture would have an advantage
  - With the caveat that the 100G FEC is KR4 and the 400G FEC is KP4
- But do people only care about 4x100GbE breakout, or do they also care about 16x25GbE, 8x50GbE and possibly 2x200GbE breakout in the future?
  - With the caveat that we don't know the architecture of some of these speeds
- If your port group cares about these other speeds then you need a FEC implementation that can drive FEC for all of these speeds
- One design that can accomplish this, is a single 400G FEC block that can do KP/KR FEC and time share the block
  - Other architectures are also possible

Design Complexity

- Xinyuan Wang points out the extra complexity of 1x400G vs. 4x100G is his last logic ad hoc presentation, handling the end of one block when another is starting
- This is a very small fraction of the overall logic required for the solution and in the big picture to me is a don't care

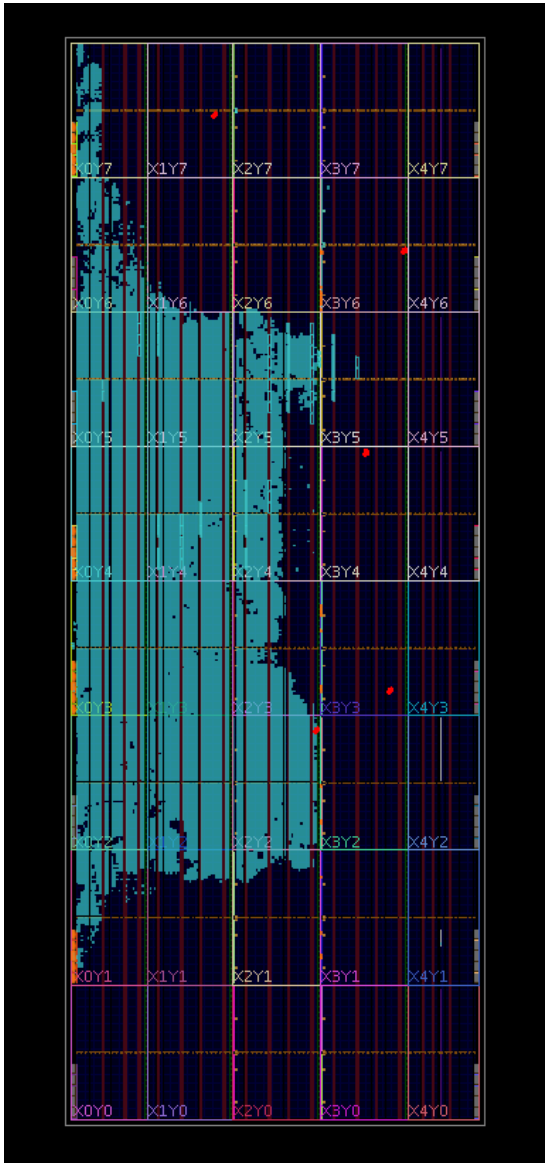
Implementation of Option 1 of Arch A:



From: wangx_01_0415_logic

Feasibility of 400G Today

- Would like to reiterate that 400G is very feasible today in existing FPGA technology
  - It has already been demonstrated (without FEC so far), but a lot of room is left to add FEC
- This is true for a 1x400G or 4x100G FEC architecture
- 4x100G KP4 FEC is a little larger but similar in size to a 1x400G FEC implementation
  - Even with breakout sizing can be very similar depending on the architecture chosen
- The picture shows a placed 400G MC/PCS in a mid size and shipping FPGA



Latency

- With a 1x400G architecture you can achieve lower latency simply because the block time is ¼ of a 4x100G architecture

Thanks!