NTT Electronics

Receiver technical feasibility and cost trends on 10-km 8x50G proposals

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Executive summary

The joint contribution, cole_3bs_01_0515.pdf, proposes 8x50G PAM4 covering up to 10 km, and this contribution provides information regarding technical feasibility and cost-trend investigation.

Generally, it is believed that NRZ 53.2Gbaud and PAM4 26.6Gbaud have pros and cons.

1) 53.2Gbaud NRZ:

Pros; better OSNR tolerance (effective for 10km)

Cons; High bandwidth requirements, high-cost implementations (e.g. packaging).

2) 26.6Gbaud PAM4:

Pros; Low bandwidth requirement resulting low-cost implementations.

Cons; worse OSNR tolerance (when using PIN-PD)

Now 25G APD is to be available in the market, which could offset the OSNR drawback of PAM4 in 10km.

Big Ticket Items for 10-km 26.6GBd-PAM4

Proposal

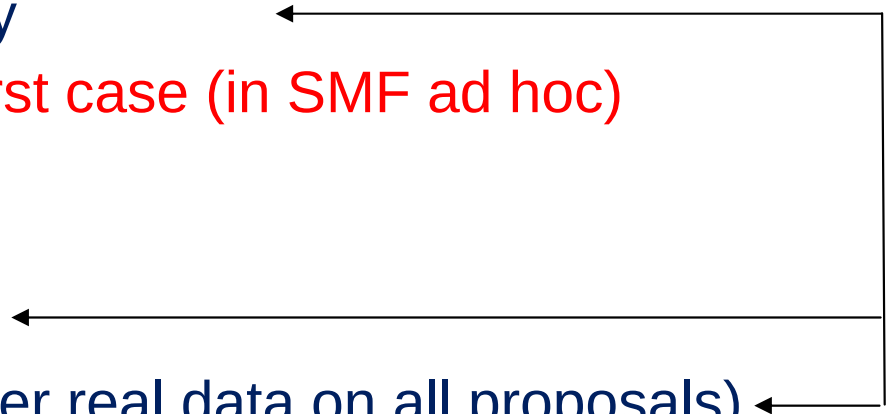
cole_3bs_02_0115.pdf (26.6 GBd PAM4)

BTI status

bti_3bs_01_0315.pdf (summary of March 2015 meeting)

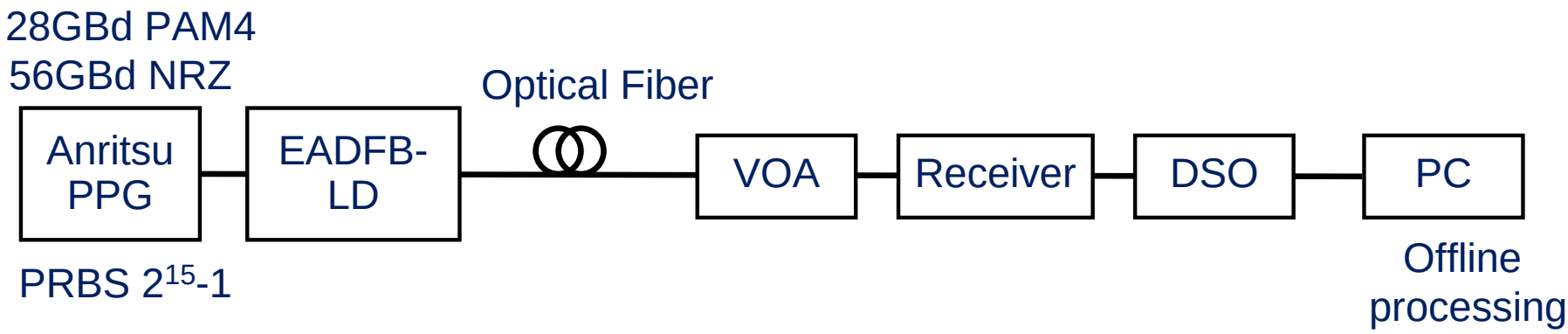
Items in red have had supporting material presented.

- Evaluate Coupling between electrical and optical interfaces
- RX Technical feasibility
- Dispersion penalty worst case (in SMF ad hoc)
- TDP
- MPI
- RX sensitivity
- More Test results (prefer real data on all proposals)



covered in this presentation

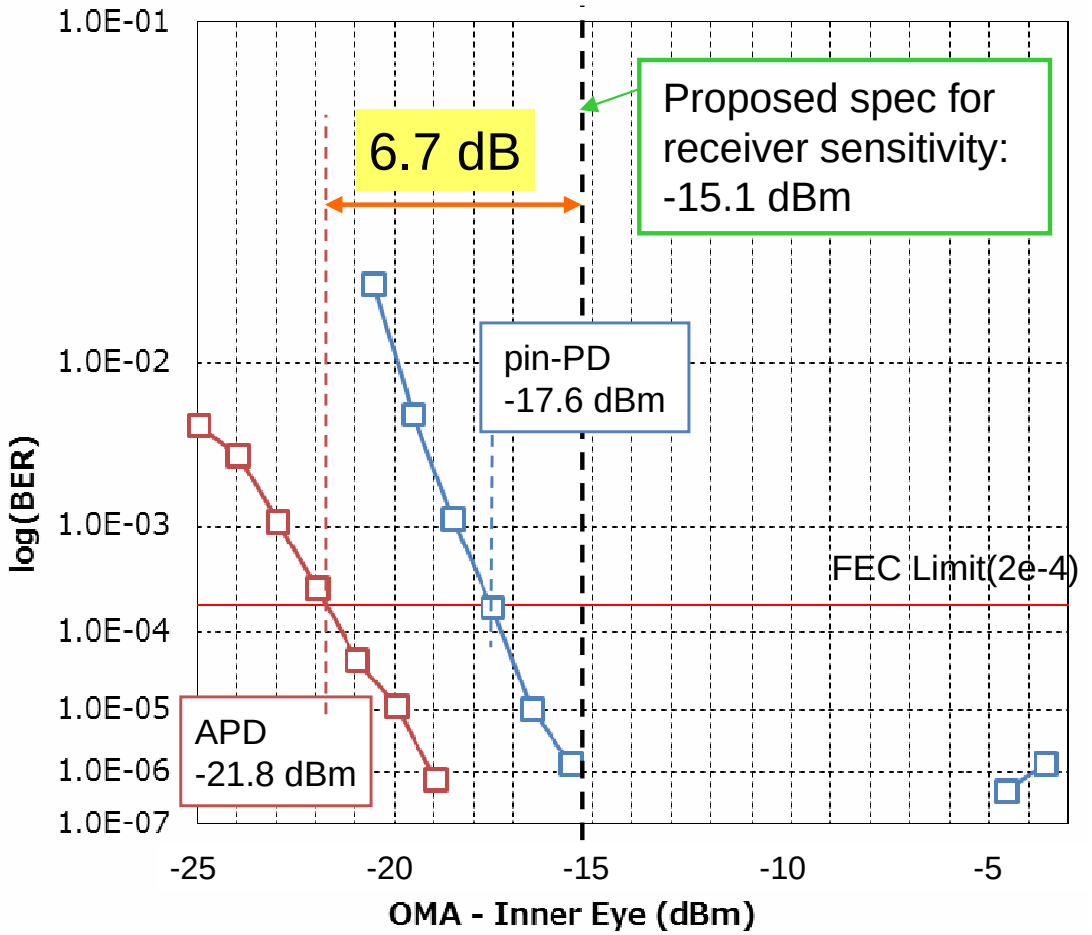
Experimental setup for 56Gb/s-PAM4, NRZ



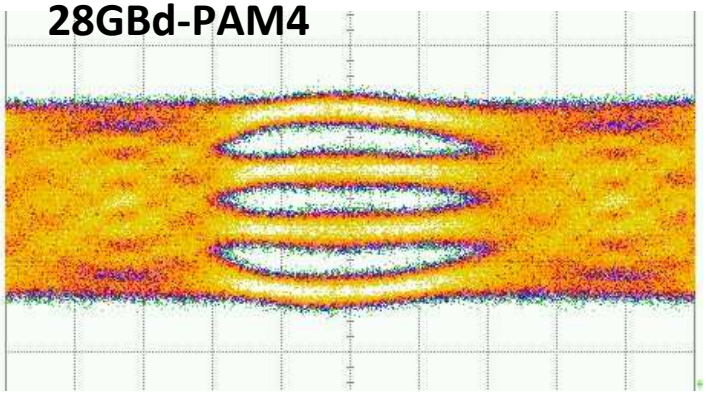
format	EADFB-LD	Receiver	DSO
28GBd PAM4	λ: 1304.34 nm BW: 31 GHz	pin-PD + Linear TIA BW: 19 GHz or APD + Linear TIA BW: 14 GHz (for PAM4), 15.5 GHz (for NRZ)	80 GS/s BW: 33 GHz
56GBd NRZ	λ: 1305.07 nm BW: 58 GHz		160 GS/s BW: 63 GHz

- Commercial grade pin-PD and APD have tested.
- To evaluate receivers, we have used EADFB-LDs with sufficient bandwidth as optical transmitter for each modulation format.

BER measurement: 28GBd-PAM4



Condition
28Gbaud PAM4/PRBS15
Vpd
pin-PD: 4 V
APD: 25.6 V
(Multiplied Responsivity ~5 A/W)
FFE: 17tap

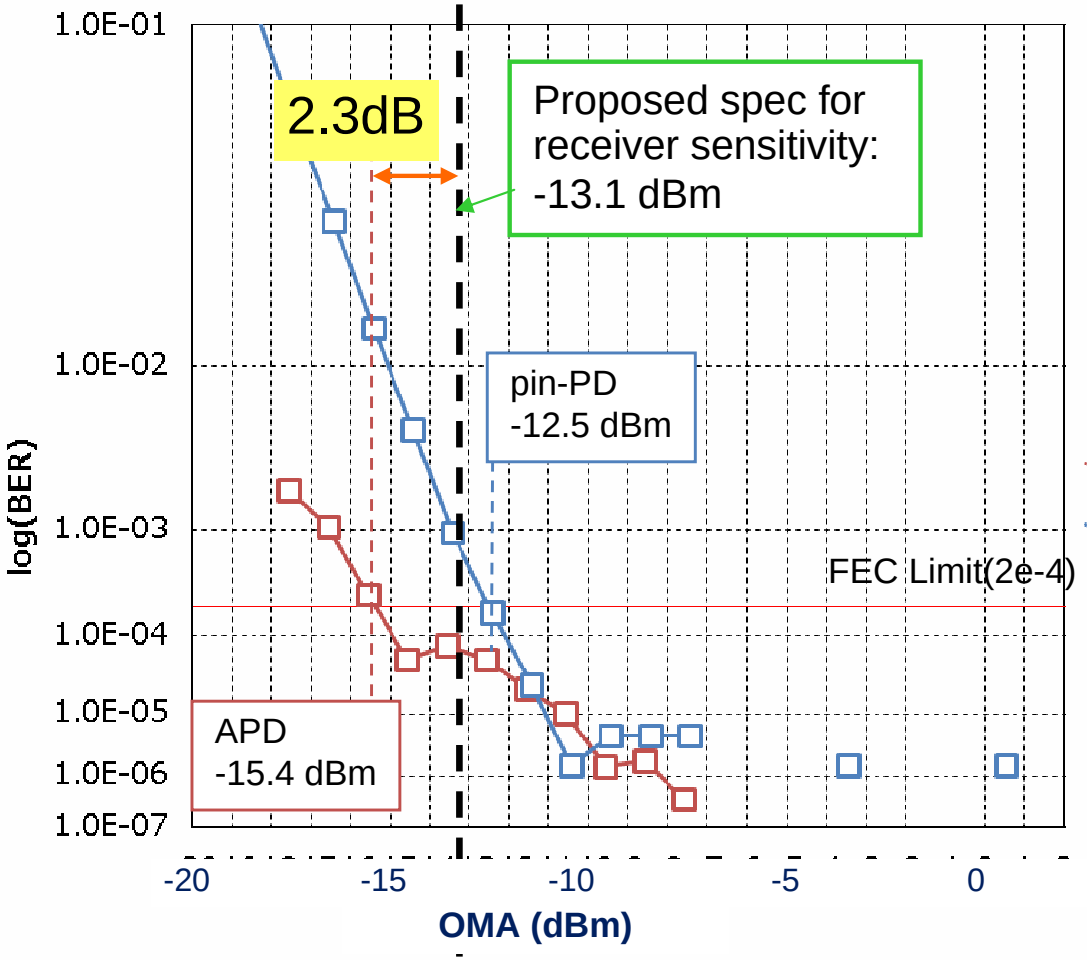


with Agilent 86116C Opt. 025

- With pin-PD, margin to required sensitivity* is not enough for production.
- APD provides enough margin of 6.7dB to the sensitivity.

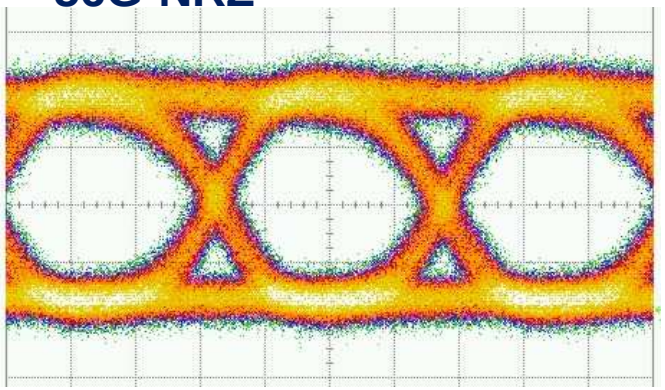
* See Appendix (slide 14)

BER measurement: 56GBd-NRZ



Condition
56Gbaud NRZ/PRBS15
Vpd
pin-PD: 4 V
APD: 22 V
(Multiplied Responsivity ~3 A/W)
FFE: 17tap

56G-NRZ



with Agilent 86116C Opt. 040

- With pin-PD, required sensitivity* could not be obtained.
- APD provides 2.3dB margin to the sensitivity.
- Insufficient bandwidth of receiver degrades BER performance.

* See Appendix (slide 14) ,

Challenges on bandwidth improvement

- Technical challenges on bandwidth improvement is necessary for 53.2Gbaud-NRZ.
- Particularly, APD has some hurdles in operating with higher baud rate.

Hurdles

- Improvement on Gain-Bandwidth product limitation
- Minimizing responsivity degradation due to high-speed configuration
- Confirmation of reliability under high-current density (small junction area)
- Lack of high-speed linear TIA array used with high-speed APD

APD technical feasibility for 50Gbps/λ

Item	26.6GBd-PAM4	53.2GBd-NRZ
APD technology	Based on 100GbE technologies	Newly developed technology is necessary.
APD performance	Current 25G-APD can provide enough margin in sensitivity with linear TIA.	Higher bandwidth should be achieved without serious gain degradation.
Reliability	Based on 100GbE technologies, and linearity reliability needs to be checked.	Expected risk : higher current density of small junction area for high-speed response.
Multi-ch. APD-ROSA	1st production in 2017	1st production in or after 2019
Multi-ch. Packaging	Based on 100GbE technologies	High-speed design, material, and interface are necessary.

Transceiver technical feasibility

From compact and multi-channel integration perspective…

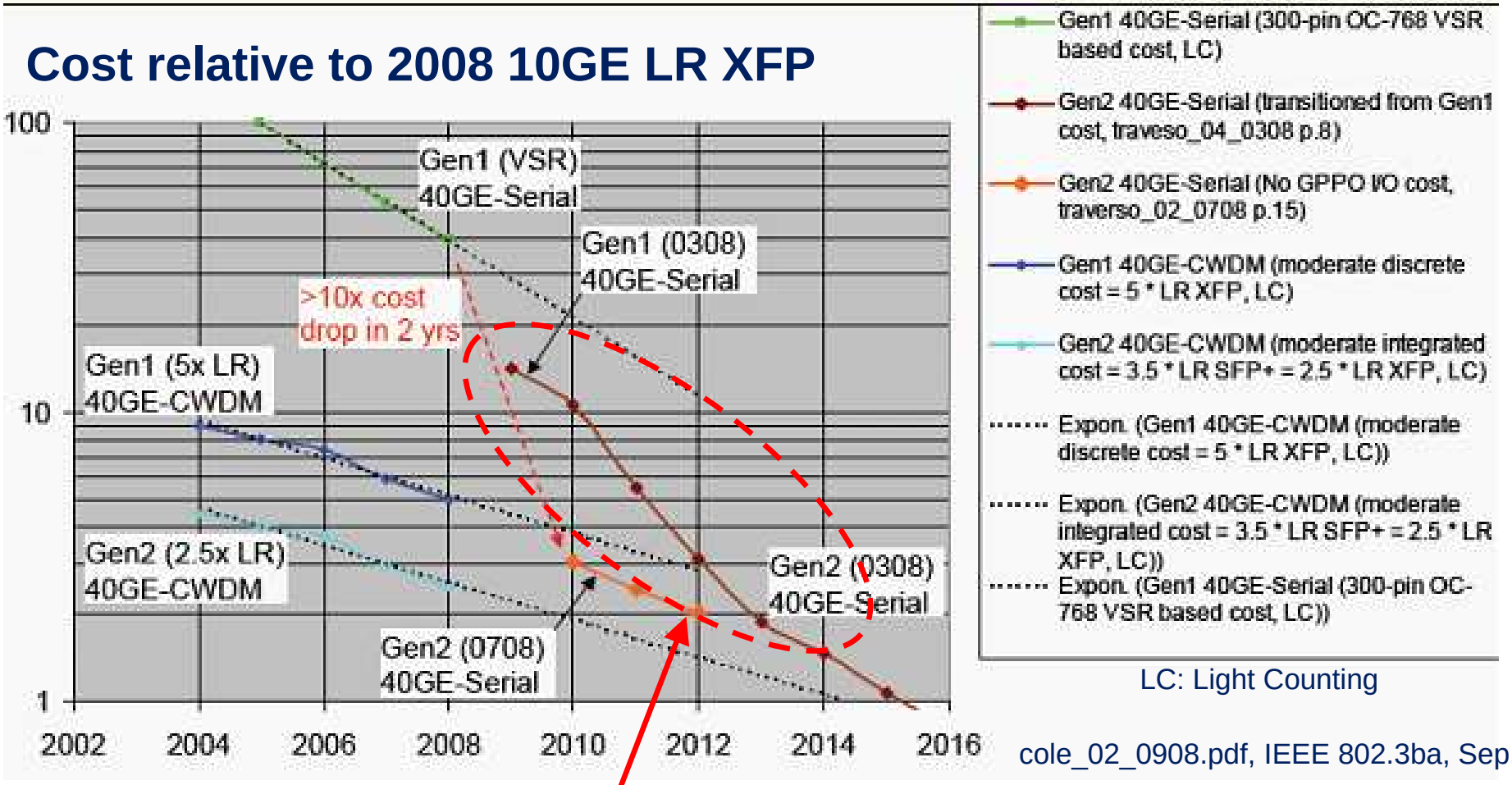
- 400GbE transceiver form factor should be CFP2 or smaller in order to achieve higher port density than that of 100GbE.
- Integrated 4- or 8- channel TOSA/ROSA must be indispensable.

	Compact multi-channel component
26.6GBd PAM4	**Components for 100GbE and 100G digital coherent can be applied.** **All components, including PHY chip, might be ready for production in 2016. Multi-ch. TOSA/ROSA and transceiver would be available in 2017.**
53.2G NRZ (w/o EQ)	**No multi-channel receiver has been reported.** **Reported demonstration[1] used single-ch XLMD with GPPO connector.** **CDR introduced. TIA and PHY chips under consideration.**
53.2G NRZ (w EQ)	**Reported demonstration[2] with 100GbE class optical device used not only FFE but also DFE. It requires large scale DSP.** **Required sampling rate for ADC might be over 80 GS/s.**

EQ: equalizer

[1] shirao_3bs_01a_0315.pdf [2] wen_3bs_01_0115.pdf

Cost trend in Ethernet market



LC: Light Counting

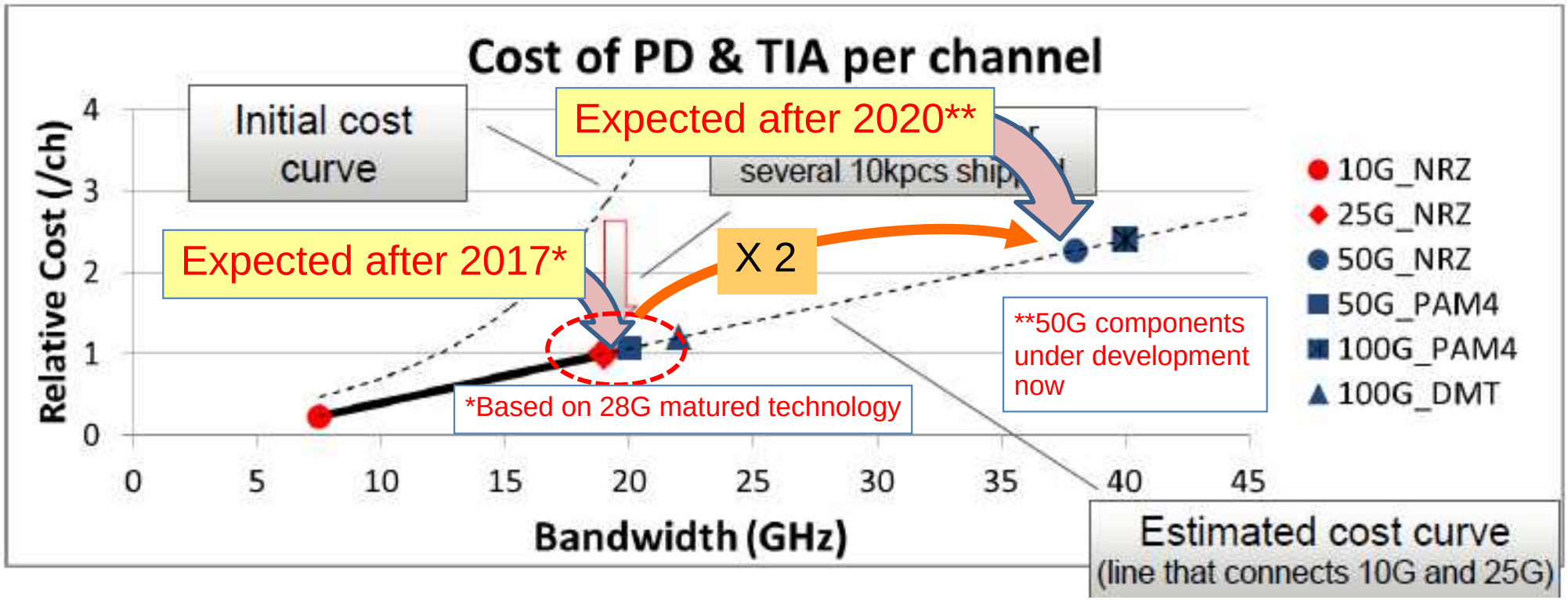
cole_02_0908.pdf, IEEE 802.3ba, Sep. 2008

High speed components require **5 years** between technology deployment start and cost/market maturity.

Cost achievement timeline

ROSA relative cost estimation

FUJITSU



isono_3bs_01a_1114.pdf

It would be hard to make 8 x 53G NRZ transceiver with proper cost in 2017.

Summary

- Rx technical feasibility and sensitivity were experimentally evaluated with production grade pin-PD or APD for 28GBd-PAM4 and 56G-NRZ.
- With pin-PD, we obtained receiver sensitivity clearing the required value for 28GBd-PAM4 though not achieving required sensitivity for 56G-NRZ. Current production APD can provide 6.7 dB margin to link power budgets for 28GBd-PAM4.
- From a viewpoint of production of multi-ch transceiver, 26.6GBd-PAM4 400GbE transceiver can be made in 2017 with proper size and cost though it seems very difficult to make 53.2G-NRZ 400GbE transceiver before 2020.

Appendix) Proposed specifications for 53.2 Gbps/λ

	53.2G NRZ (Min.)	26.6GBd PAM4 (Min.)
OMA/lane	-2.5 dBm	0.5 dBm
OMA - TDP	-3.5 dBm	-0.5 dBm
Fiber IL (10 km)	-6.3 dB	-6.3 dB
Rx in	**-9.8 dBm**	**-11.8 dBm**
DMX loss	-3.0 dB	-3.0 dB
XTalk penalty	-0.3 dB	-0.3 dB
Single PD in *	**-13.1 dBm**	**-15.1 dBm**
	cole_3bs_04_0315	cole_3bs_01_0515

* Not including MPI nor equaliser penalty

Thank you