CDAUI-8 PAM4 Reference Receiver CDR

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Supporters

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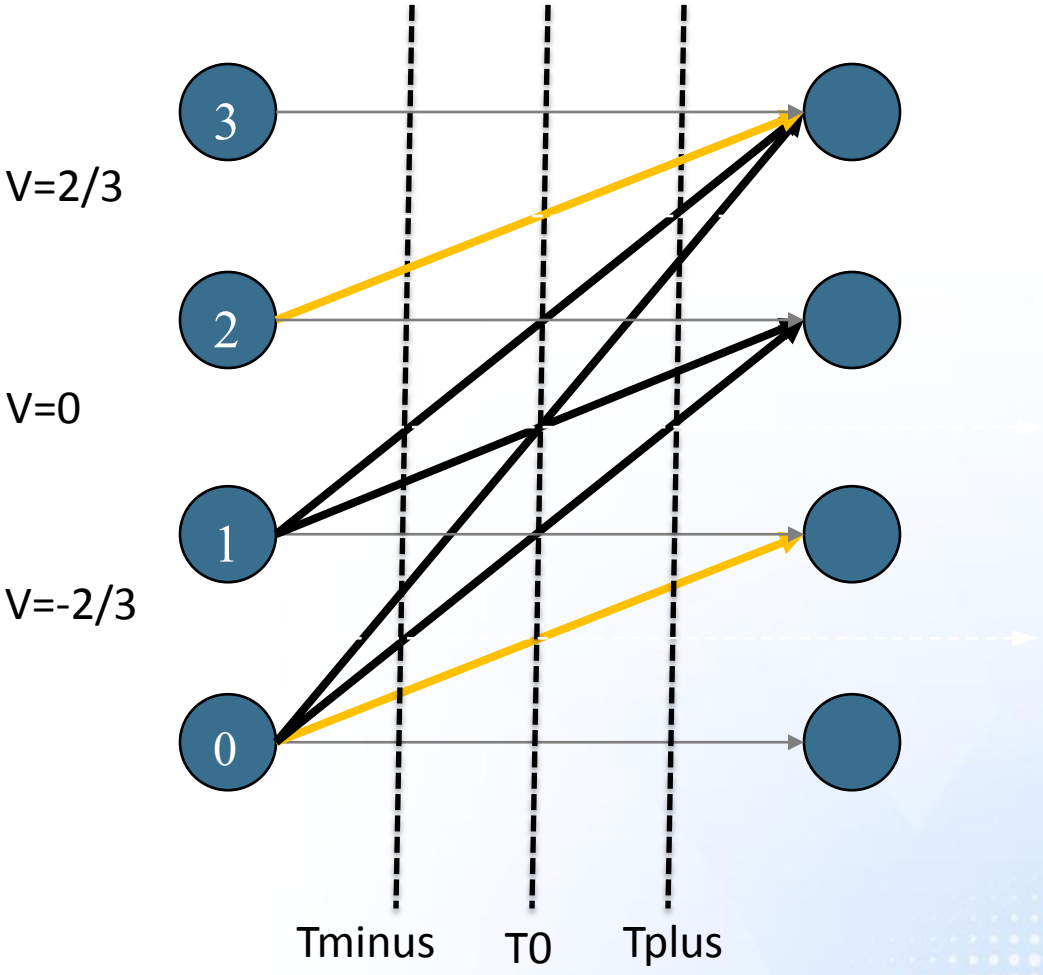
Background

- This presentation is an updated version of oif2015.184.01
- It was presented at the April OIF meeting as a proposed update for CEI-58G (PAM4) VSR & MR, and is therefore relevant for our CDAUI-8 baselines.

Introduction

- A proper measurement timing reference is critical for:
  - Rx jitter definitions
  - TX jitter definitions
- PAM4 adds new complexity
  - Data pattern affects transition density
  - Transitions are no longer only at 0V (differential)
- DSP CDR solutions common for PAM4 (versus analog)
  - Have Rx jitter bandwidth limited to 100(s) kHz
- Will propose test solution, and identify potential conflicts

PAM4 Transitions



6 rising edges
6 falling edges
4 non trans
16 options

PAM4 Transition density (td) is 12/16 = 75%

JP03A is 100% td
JP03B is ~100% td

QPRBS13 is 75% td

Test Pattern transition density

- JP03A (100%)
  - 03
- JP03B (97%)
  - 0303030303030303030303030303033030303030303030303030303030
    - 100% transitions cross 0V
- Quaternary PRBS13 (75%)
  - Approximate with random transitions
  - 75% transition density
    - 50% transitions cross 0V (some early and late)
    - 25% transitions cross ±2/3
- Transmitter linearity (6.25%)
  - 6 transitions in 160 bits cross 0v
  - 4 additional transitions at ±2/3

Reference RX CDR phase detector

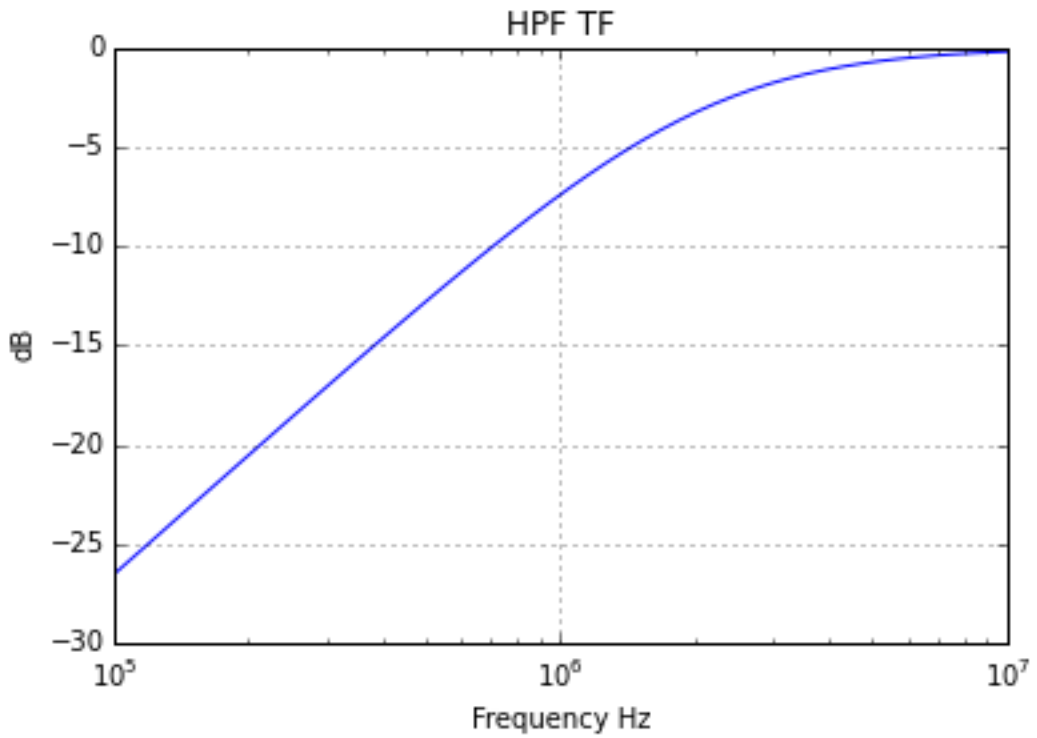
- Simplest (option “S”)
  - 1 detector: 0V crossing
  - allow all edges that cross to be counted
- More complicated (option “A”)
  - 1 detector: 0V crossing
  - Restrict data to symmetric data
  - 03--30 or 12--21 transitions
- More complicated (option “B”)
  - 3 detectors: -2/3, 0, 2/3
- Full Monty (option “F”)
  - 5 detector: -2/3, -1/3, 0, 1/3, 2/3

DSP based versus Analog Receiver

- DSP CDR receiver:
  - Uses voltage samples
  - 1UI time spaced
  - Can use all transitions as information
  - Essentially ignores edge timing
  - Requires processing time for CDR updates (160kHz for KP4)
- Analog CDR receiver:
  - Have limited slicing thresholds
    - Simplest is one at 0v
  - Often 2x oversampling (measuring edge timing)
  - Have relatively high loop bandwidths (10MHz for CAUI-4)

KP4 TX Jitter Generation HPF

- Measurement bandwidth is 2MHz and up.
- $G(f) = f / (f - jf_n e^{j2\pi T})$
- $f_n = 2.12$ MHz
- $T = 0.0286$ µs



KP4 Rx Jitter Tolerance

Description	Point 1	Point 2	Point 3 (Implied)	Unit
Jitter Frequency	16	160	1600	kHz
Jitter Amplitude	5	0.5	0.05	UI

KP4 receiver limits jitter beyond 160kHz but
only measures TX jitter beyond 2MHz

Implied specification is 0.05 UI Sinusoidal Jitter tolerance past 1600kHz (1.6MHz)
Note: only points 1 and 2 are in the compliance table.

Detailed proposal statement(s)

- Should the Tx jitter generation budget be:
  - Measured by a physical CDR with phase detector (S,A,B,F)
  - → Propose S. (simple test equipment exists)
- Should the Rx jitter tolerance calibration be:
  - Measured by a physical CDR with phase detector (S,A,B,F)
  - → Propose S. (simple test equipment exists)
- Should TX jitter generation HPF and Rx tolerance LPF be coupled?
  - → Propose yes.
- What should the BW be?
  - Propose 320kHz at 0.5 UI (2x 160kHz).
  - Bandwidth measured with QPRBS13 pattern
  - **Enables both DSP and analog CDR**