100Gb/s/Lambda PAM4
Status of BTIs

Alan Tipper Semtech
Vipul Bhatt InPhi
Brian Welch Luxtera
Gary Nicholl Cisco

Supporters

- Will Bliss, Broadcom
- Matt Brown, Applied Micro
- Keith Conroy, Multiphy
- Ian Dedic, Socionext
- Riu Hirai, Hitachi
- Nobuhiko Kikuchi, Hitachi
- Dave Lewis, JDSU
- Mark Nowell, Cisco
- Vasu Parthasarathy, Broadcom
- Bharat Tailor, Semtech
- Atsushi Takai , Oclaro
- Kohichi Tamura, Oclaro
- Ed Ulrichs, Source Photonics
- Winston Way, Neo Photonics

100G/lambda PAM4 BTIs

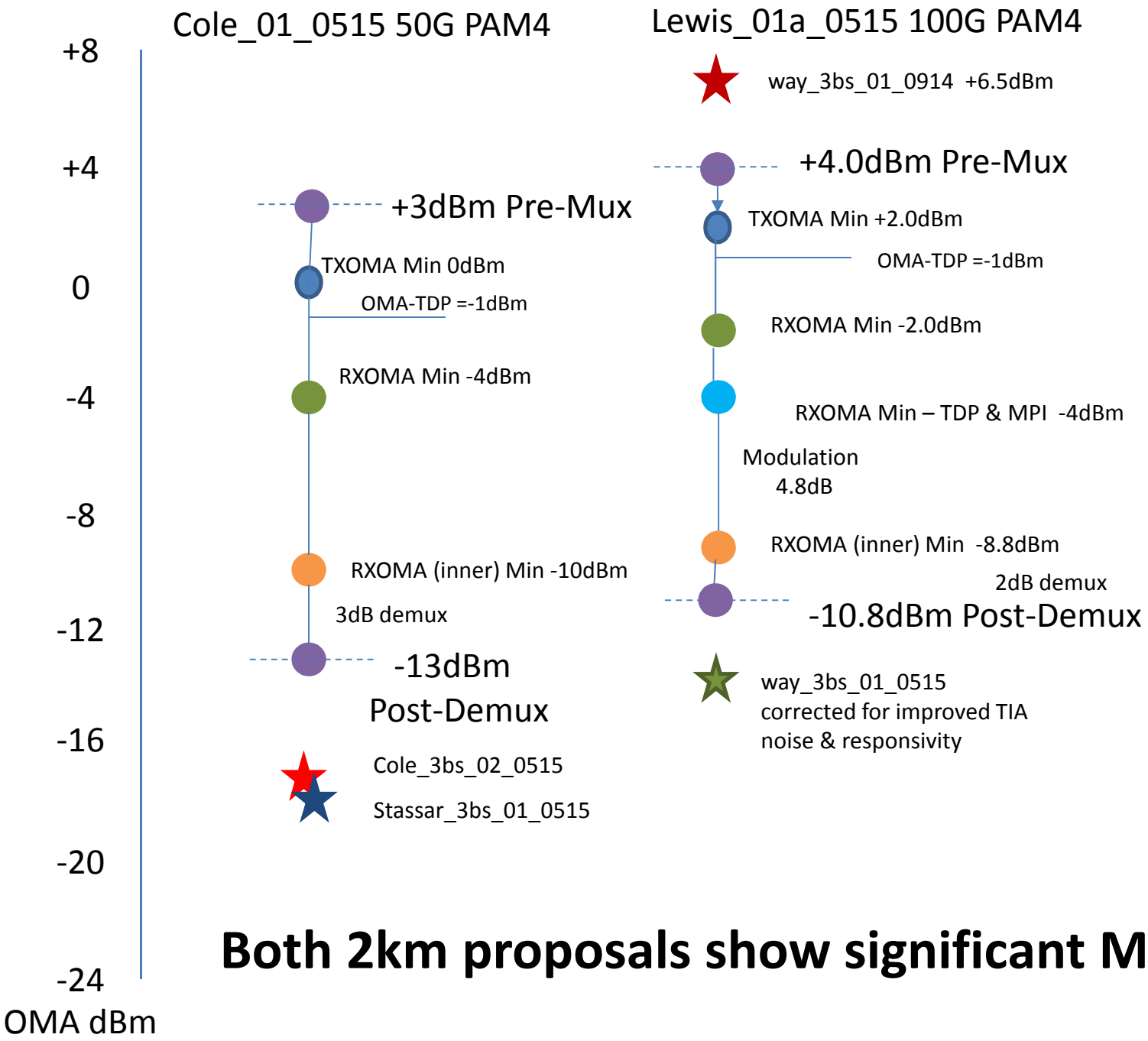
- Electrical & Optical Modulation match
  - For CMOS implementations there is no Power/Area advantage in coupling Electrical and Optical modulation szczepanek_3bs_01a_0315
- Availability of High Bandwidth Components
  - Optimal Tx BW 31GHz & Rx BW ~ 28GHz zhu_3bs_01_0714, Experiments with these BW way_3bs_01a_0115
  - 30GHz TIA feasible based on industry trends tipper_3bs_01_0315
  - 4 candidate 56Gbaud PAM4 modulators presented at OFC 2015 TU2A2, Th3A3, Th3A4 ,Tu2A5
- Dispersion
  - Negligible CD penalty with RX EQ, <0.3dB without EQ tipper_3bs_01_0315
    - Previous Measurements of 53Gbaud NRZ & 28Gbaud PAM4 do not suggest a 53 Gbaud PAM4 dispersion issue at +6.7ps/nm to -11.9ps/nm shirao_3bs_01a_0315, stassar_3bs_01a_0315
    - Way_3bs_01_0515 demonstrates experimentally <0.1dB dispersion penalty at 56GBd across +6.9ps/nm to -12ps/nm

TIA NEP Performance

- TIA performance is determined by a trade-off among bandwidth, noise, power dissipation, process technology, and design optimization.
- TIA suitable for 25 GBaud operation can currently achieve NEP value of well under 20 pA/sqrt-Hz, with some achieving NEP value of under 15 pA/sqrt-Hz.
- We estimate that TIA suitable for 50 GBaud operation will be able to achieve NEP value of under 23 pA/sqrt-Hz by managing the trade-off mentioned above.
  - This is consistent with lewis_3bs_01_0515 link budget and tipper_01_0215_smf modelling.

Lab based tests should be interpreted using realistic receiver specifications **not legacy instrumentation devices**

- Instrumentation Rx: 30 – 40pA/rt Hz and low responsivity
- Product '*capability*' for 30GHz BW class TIAs is much better than this
  - Cole_02_0515 16pA/rt Hz 27 GHz limiting Rx
  - Takai_01_0515 20pA/rt Hz 56GBaud NRZ Rx
  - Current 20GHz linear Rx designs achieve <15pA/rt Hz
  - Tipper_01_0315 industry trend for 30GHz linear Rx ~23pA/rtHz
- Use 23pA/rt Hz as a working assumption linear for 53GBaud PAM4 product Rx



Both 2km proposals show significant Margin

Not ‘BTIs’ but recurring themes…

- Error Floors
  - Lab measurements showing gradual improvements over subsequent meetings
  - ADC Noise, EA driver SNR main causes of error floor tipper_3bs_01a_1114, way_3bs_01a_0115
  - Measured Error floors replicated on simulation way_3bs_01a_1114
  - No errors in 10^6 bits demonstrated at 60GBd in Conroy_3bs_01_0515
- SSPR Pattern Penalty
  - No SSPR pattern penalty experimentally confirmed for LF cut < 100kHz way_3bs_01a_0115
- Feasibility of DSP
  - ADC BW > 18GHz DAC BW> 16.5 GHz Required way_3bs_01a_0115
  - Socionext & IBM ADC feasibility papers presented at OFC 2015 Tu1B2, M1B 18GHz BW, 53GSa/s well within capability
  - InPhi presented feasibility of 56GBaud PAM DSP at OFC 2015 W4H4
  - Multiphy presented feasibility of 56Gbaud PAM4 at OFC 2015 Th2A.67
  - Semtech presented feasibility of DSP based equalization of electro-optic packaging interconnects at OFC 2015 W4H6
- Cost
  - 2x cost advantage over cooled 8 x 50G PAM4 Yu_3bs_01b_1114
  - 3.3x cost advantage over cooled 8 x 50G NRZ Yu_3bs_01b_1114
  - 2.3x cost advantage over 8 x 50G welch_3bs_02a_0115
- Power Consumption
  - 1.5 (1.4) x less power than cooled 8 x 50G NRZ (PAM4) isono_3bs_01a_1114
  - 1.2 (1.5) x less power than cooled 8 x 50G NRZ (PAM4) rao_3bs_01a_0115
  - 1.2x less power than cooled 8 x 50G NRZ rao_3bs_01a_0115
  - 1.3x less power than 8x50G NRZ or PAM welch_3bs_02a_0115

Summary

- Broad Industry Consensus supporting 100G PAM4 proposals
  - Optics/PMD/ASIC/Module/System vendors represented
- All issues raised at previous meetings have been successfully addressed by simulation and experiment
  - Dispersion/Noise/Error floors/Signal Processing all understood
  - High Confidence in 100G PAM4 Feasibility
- 100G PAM4 Proposals reflect the lowest Power, lowest cost feasible solutions.