FEC Performance over PAM4 links with Bit-multiplexing

Tongtong Wang-Huawei

Ali Ghiasi- Ghiasi Quantum

Xinyuan Wang-Huawei

IEEE 802.3bs 400 GbE Task Force

Introduction and Background

- General consideration for PMA scheme:

  PMA scheme is key item in discussion which is related to both FEC architecture choice and PMD selection

  - Feasibility of FEC architecture
  - Provide FEC performance over optical link and electrical links
  - Potential features
    - Compatibility considerations
    - Enabling breakout. etc.

- The decision tree in selecting 400GbE FEC

  - Bit muxing or Symbol muxing
  - Implement 4x100G FEC or 1x400G FEC Architecture
    - FOM (FEC Orthogonal Multiplexing) or Non-FOM?

Why Bit Multiplexing?

- In 802.3ba/HSSG OTN support incorporated into PAR criteria
  - http://www.ieee802.org/3/ba/public/may08/trowbridge_01_0508.pdf
- 100GBase-R PMA based on bit mux allow supporting to Ethernet and OTN applications with common optical module
    - Ethernet module operates 25.78 GBd
    - OTN module operates at 27.95 GBd
- Since 802.3ba the shortcoming of bit coupled with DFE receiver could result in MTTFPA
- FEC Orthogonal Multiplexing (FOM) delivers comparable FEC performance by preserving traditional bit mux PMA to allow building common Ethernet/OTN modules

KP4 FEC Performance on PAM4 Links

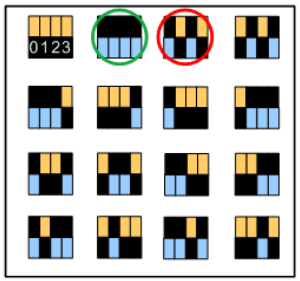
- Continue on previous analytical procedure in “wang_t_3bs_01a_0315” with two modifications:

  - Error propagation parameter is 0.75 instead of 0.5 as for NRZ, that means more probabilities for longer burst errors. (assuming initial error corrupts either MSB or LSB, not both bits)

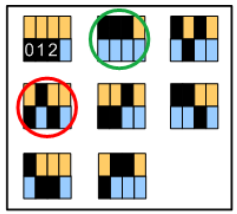
  - Reconsider all PAM4 error patterns for 2-17 symbol long burst errors and quantify the probability for each pattern to evaluate the FEC performance with Non-FOM bit mux

PAM4 Error Patterns for Single Signal Level Transition Error

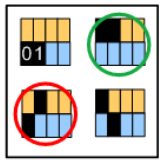
- 4/3/2 PAM4 symbol correlated error have following error patterns:



Error patterns in 4 symbol burst error



Error patterns in 3 symbol burst error



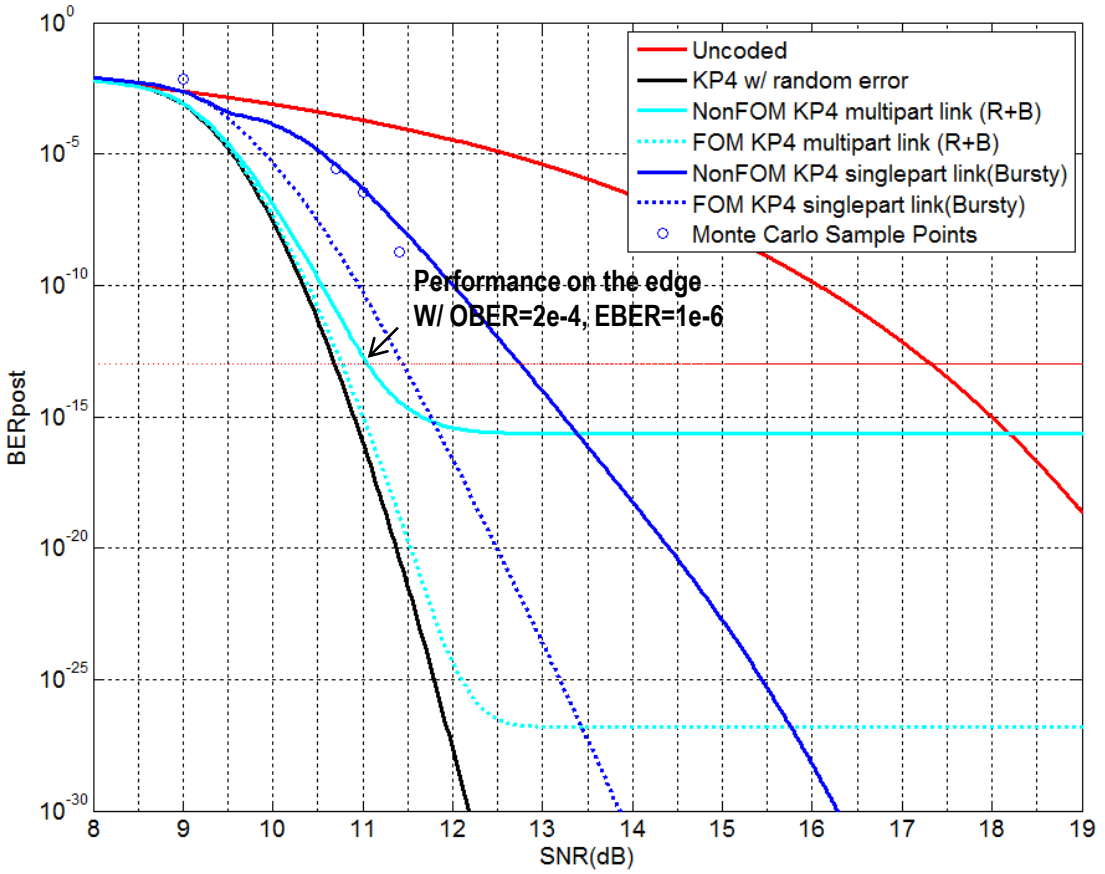
Error patterns in 2 symbol burst error

- Each error pattern has different impact on FEC Performance

  - For example, the left error pattern will cause 1 symbol error by 35% and 15% 2 symbol error in FOM bit mux
  - Red circle in diagram indicates the worst case for FOM bit muxing, green circle for nonFOM bit muxing

KP4 FEC Performance on PAM4 Links

- For PAM4 links, FEC performance with FOM bitmux is better than Non-FOM bitmux, same as for NRZ links
- Error Floor exists on multi-part links, assuming BER on electrical links is 1e-6*,
  - ~1e-16 with Non-FOM scheme
  - ~1e-25 with FOM scheme
- Multi part links in this evaluation assume random error on optical links and burst errors on electrical links.



*To account for burst errors, this value should multiplied by 4 when a = 0.75

KP4 FEC Performance on PAM4 Links

(- for Burst + Random multi part link)

Physical input BER requirement with Non-FOM and FOM bit mux

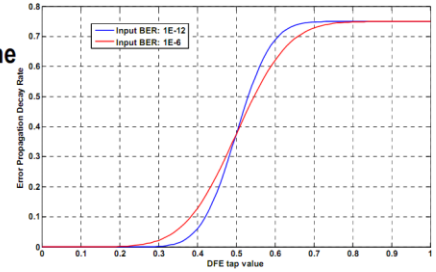
	BERpost = 1E-13 with KP4 FEC			
	Electrical Link		Optical Link	
Non-FOM Bit mux with 0.1dB optical link penalty	Burst	4.00E-06	Random	2.00E-04
FOM Bit mux with 0.1dB optical link penalty	Burst	8.00E-05	Random	2.00E-04
FOM Bit mux with ~0.01dB optical link penalty	Burst	1.60E-05	Random	3.00E-04

- Risks on Non-FOM bit mux:
  - Limitation on optical links that no correlated error or burst error ever exist
  - BER requirement for both optical and electrical links are quite on the edge, without much margin
- FOM bit mux has better performance than Non-FOM, which makes system more robust and enable more PMD features

Risk 1: Error Propagation of PAM4 DFE

- PAM4 DFE burst errors and "Error propagation Decay Rate" vs "DFE Tap Values"

- **DFE's are well known to multiply errors in the feedback loop**
  - A single error will become a burst error
- **Consider PAM4 1 tap DFE with tap coeff = 1**
  - If previous decision is wrong, then there is 3/4 probability of making a successive error
  - i.e. Probability of K consecutive errors = $(3/4)^k$
- **Lower 1st DFE tap between 0.6 to 1 have similar burst length as tap coefficient of 1**
  - Tap of 1: 0.75^k
  - Tap of 0.7: 0.72^k
  - Tap of 0.6: 0.62^k
- **A single random error may consume multiple Reed Solomon symbols**
  - Burst error coding gain is lower than coding gain for random errors



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- Multi-Tap DFE scheme is defined in PAM4 CDAUI-8 C2C channel of 400GbE

CDAUI-8 c2c Channel Spec: COM (II)

Number of signal levels	L	4	—
Level separation mismatch ratio	R_{LM}	0.92	—
Transmitter signal-to-noise ratio	SNR_{TX}	31	dB
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	5	UI
Normalized DFE coefficient magnitude limit for n = 1 for n = 2 to N_b	$b_{max}(n)$	1 0.2	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.02	UI
One-sided noise spectral density	η_0	5.2×10^{-8}	V^2/GHz
Target detector error ratio	DER_0	10^{-6}	—

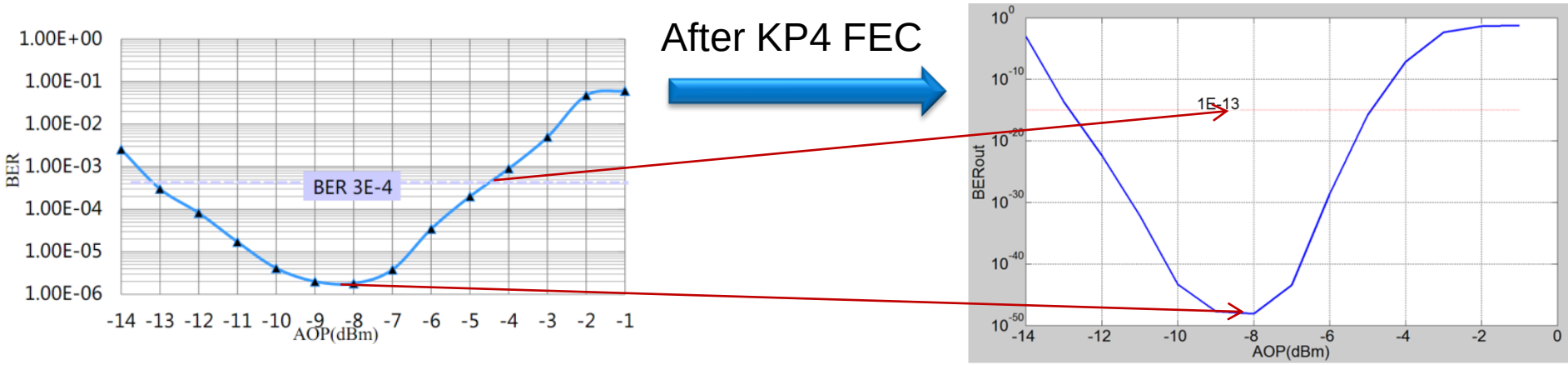
* Updated to be aligned/consistent with *healey_3bs_01_0315*

li_3bs_01a_0315

- Since error propagation factor for multi-tap DFE will cause burst error more often and it is more complex to quantify, so we assume a=0.75 as a general assumption for error decay rate.

Risk 2: Small BER Margin Cause Big Difference after FEC

- In "wang_x_3bs_01a_1114", the relationship of input BER and post BER with KP4 FEC is depicted



- Take KP4 FEC as example, 3E-4 input BER will result in post BER of ~1E-13, and 1E-6 input BER leads to post BER of ~1E-50. As illustrated small change in the input BER can result in very large change in post BER
- For Non-FOM bit mux PMA, there isn't sufficient margin to operate 4 CDAUI links at ~3E-6 or 4E-6 BER with KP4 FEC

Risk 3: Assumption of Random Error Only in Optical Link?

- Current assumption is that “burst error only occur on electrical links” and “random error occur only on optical links”, below are few examples to illustrate scenario where burst error may occur on optical links:
  - The optical link just like electrical link may have DFE/MLSE receiver
  - Dynamic power supply noise coupled could exceed PLL tracking range
  - DC blocking caps low frequency cut off and DC wonder coupled pattern dependence
  - Compression and non-linear response of Optical-Electronic devices coupled with long data transition
  - Any optical or electrical crosstalk
- High order modulation is more sensitive to noise and further work needed to evaluate the impact to FEC/MTTFPA.

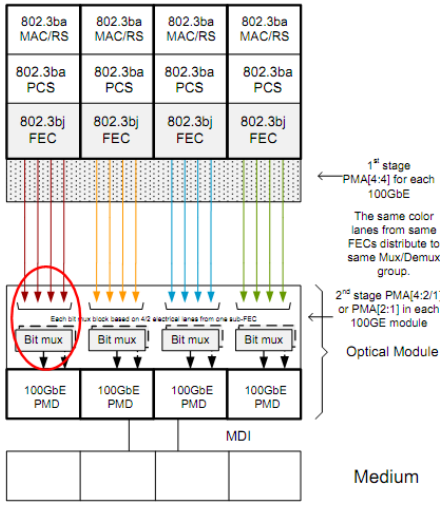
FEC Performance in Break Out 4X100GE

- "wang_x_3bs_01_0714" presented an option to enable 4x100GE breakout with 4x100G FEC architecture
- While 4x100G FEC with FOM bit mux provides good performance for 400GbE, each 100G FEC is sufficient for 100G Non-FOM bit mux breakout

- Taking 8X50G PAM4 PMD as example, 400GbE use 8:1 optical Mux/DeMux@3.5dB, while 100GbE use 2:1 optical Mux/DeMux@1.5dB. Due to insertion loss difference, each 100G FEC Performance with Non-FOM bit mux is possibly sufficient in breakout cases.
- FEC/BER performance of Non FOM bit mux with "Burst+Burst" link will be investigated

③: How to do Mux/DeMux in ¼ slice PMA of 400GbE after breakout?

- As RS FEC is mandatory in 802.3bj/bm, but how to do Mux/Demux in gearbox is undefined?
  - Option 1: General solution with Non-FOM symbol Multiplexing. No supporting bit multiplexing!
  - Option 2: FOM bit mux
    - Use 4X25Gbps RS FEC. This will un-compatible with 802.3bj/bm architecture and introduce additional latency.
    - Bit multiplexing between contiguous codeword of each 802.3 bj/bm RS FEC. This will lead to additional 100ns latency and complexity.
  - Option 3: Non-FOM bit Mux
    - Assuming low burst error probability
    - May have worse performance than FOM bit mux. However, 100GbE requires 1/10 BER objective as in 400GbE. (1e-12 vs. 1e-13)



- This Mux/DeMux feature probably will be further defined in future 100GbE standard with new PMD.

Conclusion

- From the perspective of FEC performance, 4x100G FEC supports FOM bitmux, provides larger margins for both electrical link and optical links, enable DFE usage in all PMDs(PAM-n and others)

- 4x100 FEC architecture enable 4 x 100GbE breakout with adequate FEC performance on each 100GbE instance

Thank you