FEC performance with PAM4 precoding

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Introduction

anslow_3bs_03_0515 analysed the performance of RS(544,514) FEC assuming the use of PAM4 with DFE for CDAUI-8.

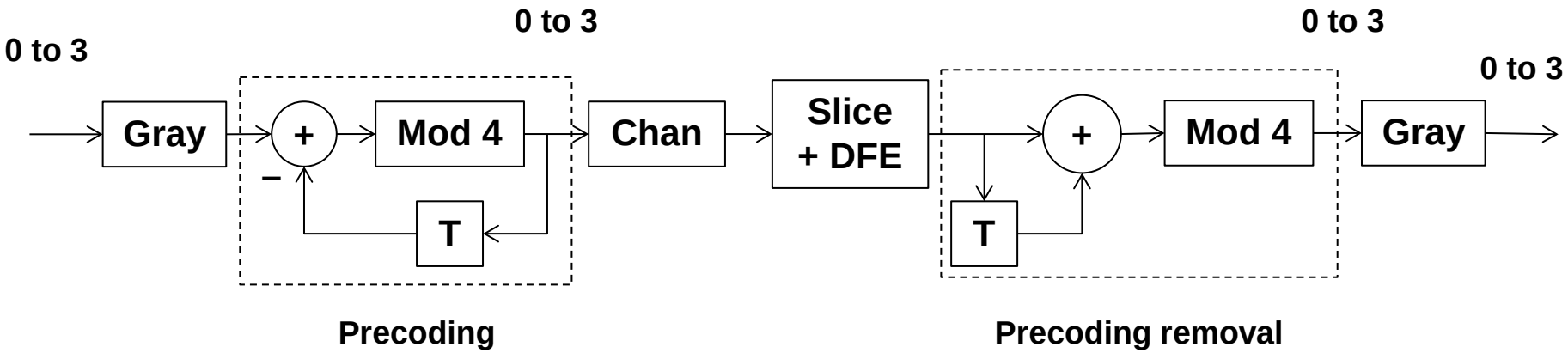
The above presentation prompted questions as to the effect that precoding such as that shown on pages 4 and 5 of parthasarathy_01_0911 would have on the FEC performance.

This presentation therefore contains analysis of the effect of precoding on the FEC performance in multi-part links.

As per previous presentations, the analysis is performed using both Monte Carlo and analytical methods.

Precoding

Precoding as defined in 94.2.2.6 for 100GBASE-KP4 was assumed. This is performed as illustrated below.



See page 5 of [parthasarathy_01_0911] for a worked example.

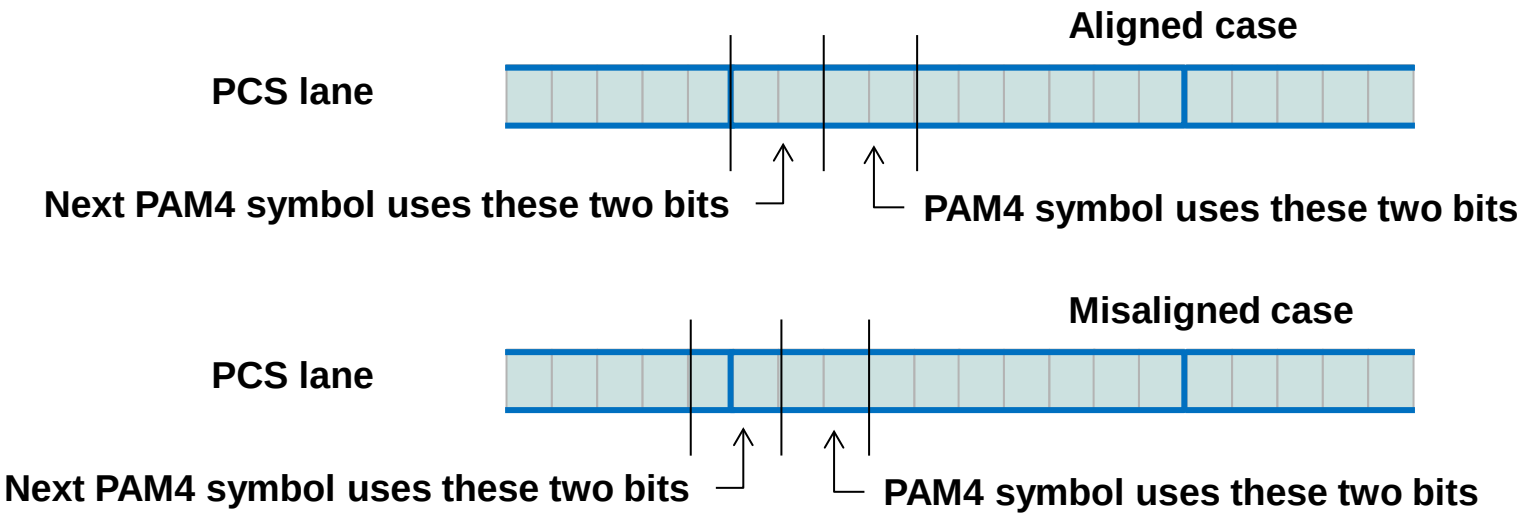
A drawback of this precoding process is that a single random errored PAM4 symbol at the slicer output turns into two errored PAM4 symbols after the precoding is removed.

Signal structure

As previously, the PCS structure in gustlin_3bs_02a_0515 is assumed with 16 PCS lanes formed by striping in 10-bit blocks aligned with the RS 10-bit symbols.

Also assume a 1 x 400G FEC architecture with the advantage of diluting the errors from the worst lane with 15 other lanes rather than with 3 other lanes for the 4 x 100G case (see anslow_3bs_05_0715).

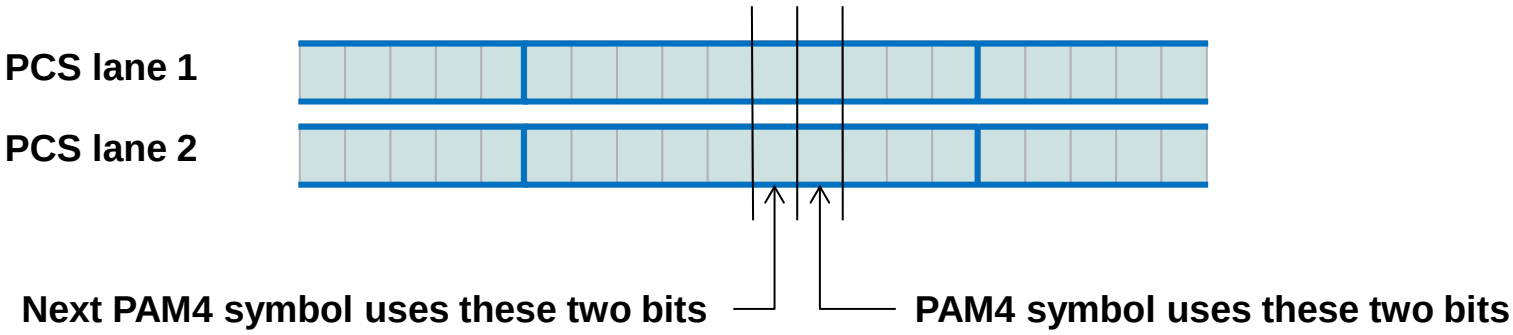
Form the PAM4 symbols two bits at a time from a single 26.5625 Gb/s PCS lane:



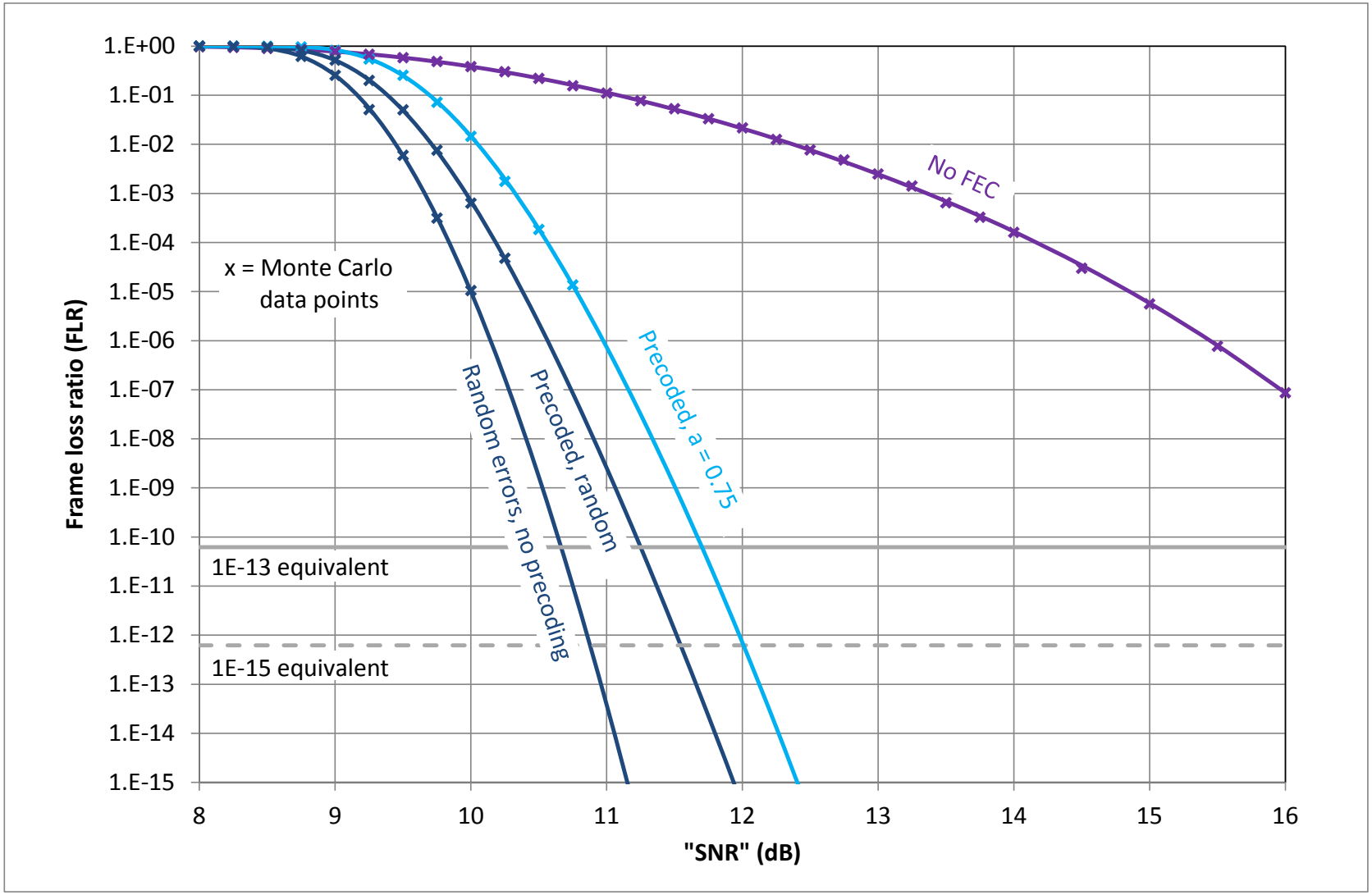
Interleaved case

In the case where a pair of 25 Gb/s PCS lanes is used to form a 50 Gb/s PAM4 lane, if FEC symbol interleaving is used, then the performance will be as for the non-interleaved case on the previous slide.

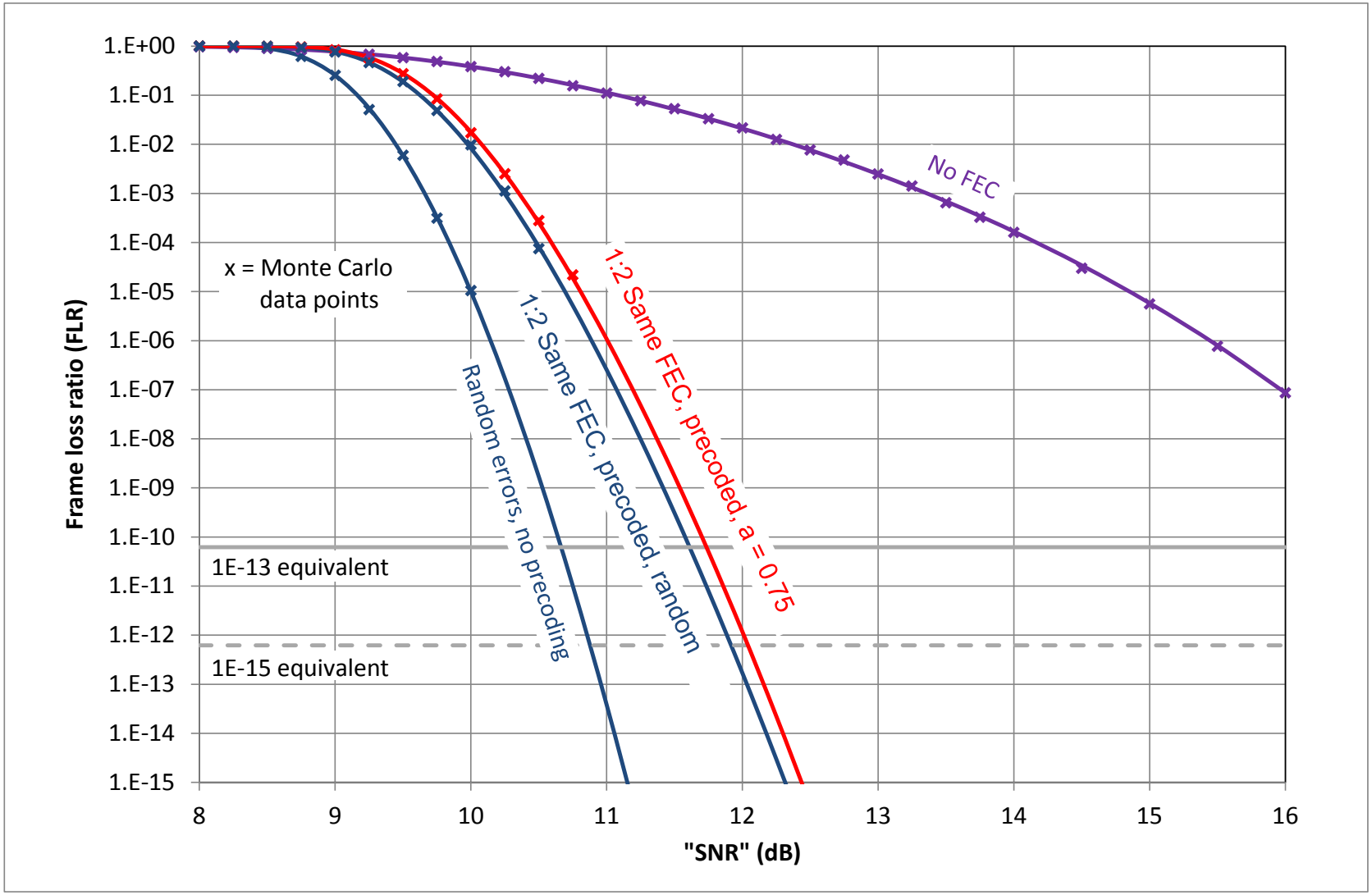
For bit interleaving, form the PAM4 symbols by taking one bit from each of the two 26.5625 Gb/s PCS lanes (as in anslow_3bs_03_0515 skew between the lanes does not change the performance for the precoded case):



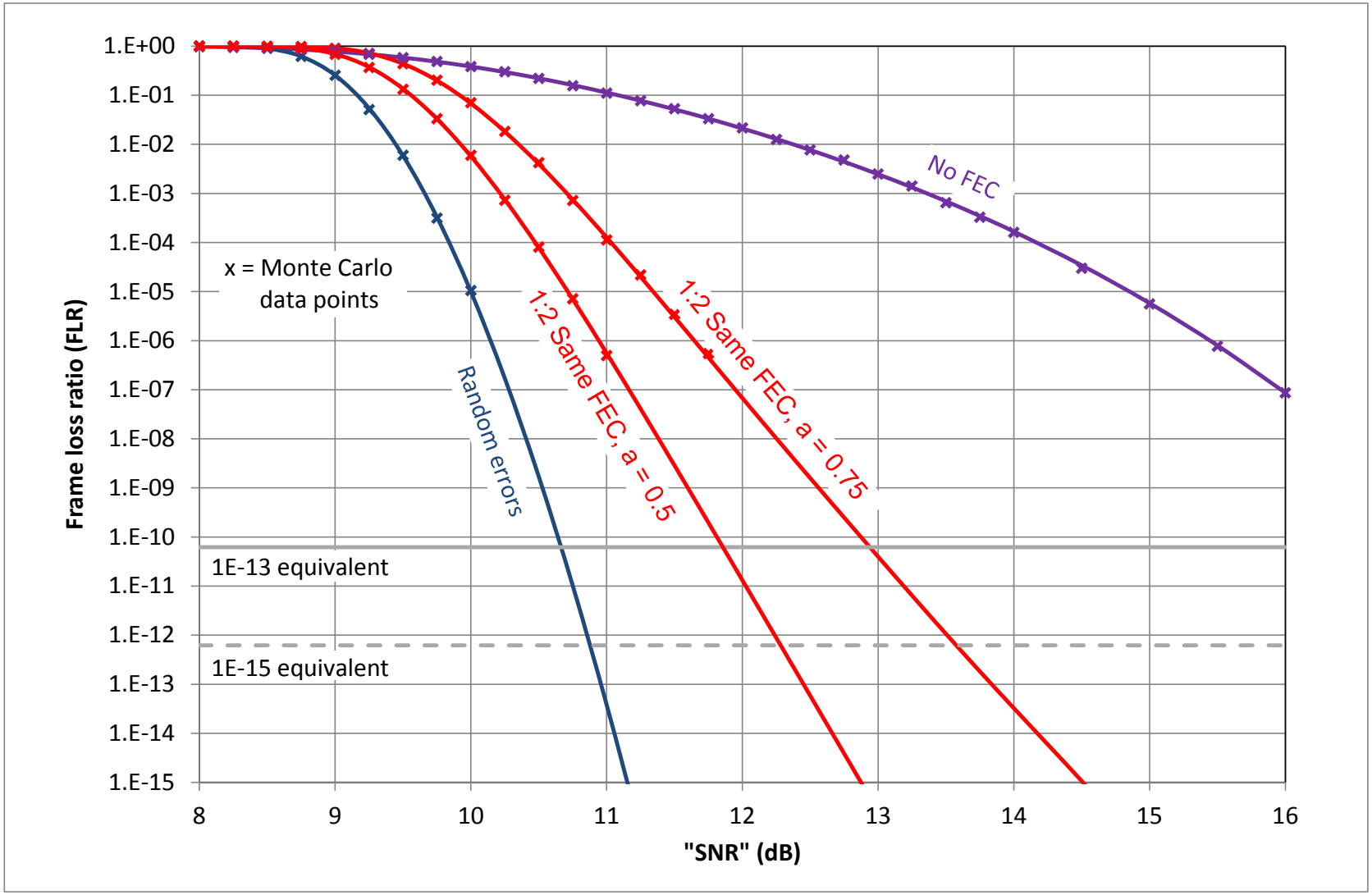
RS(544,514) results with precoding



RS(544,514) 1:2 results with precoding



RS(544,514) 1:2 results no precoding



Results for RS(544,514) all gain used for PAM4

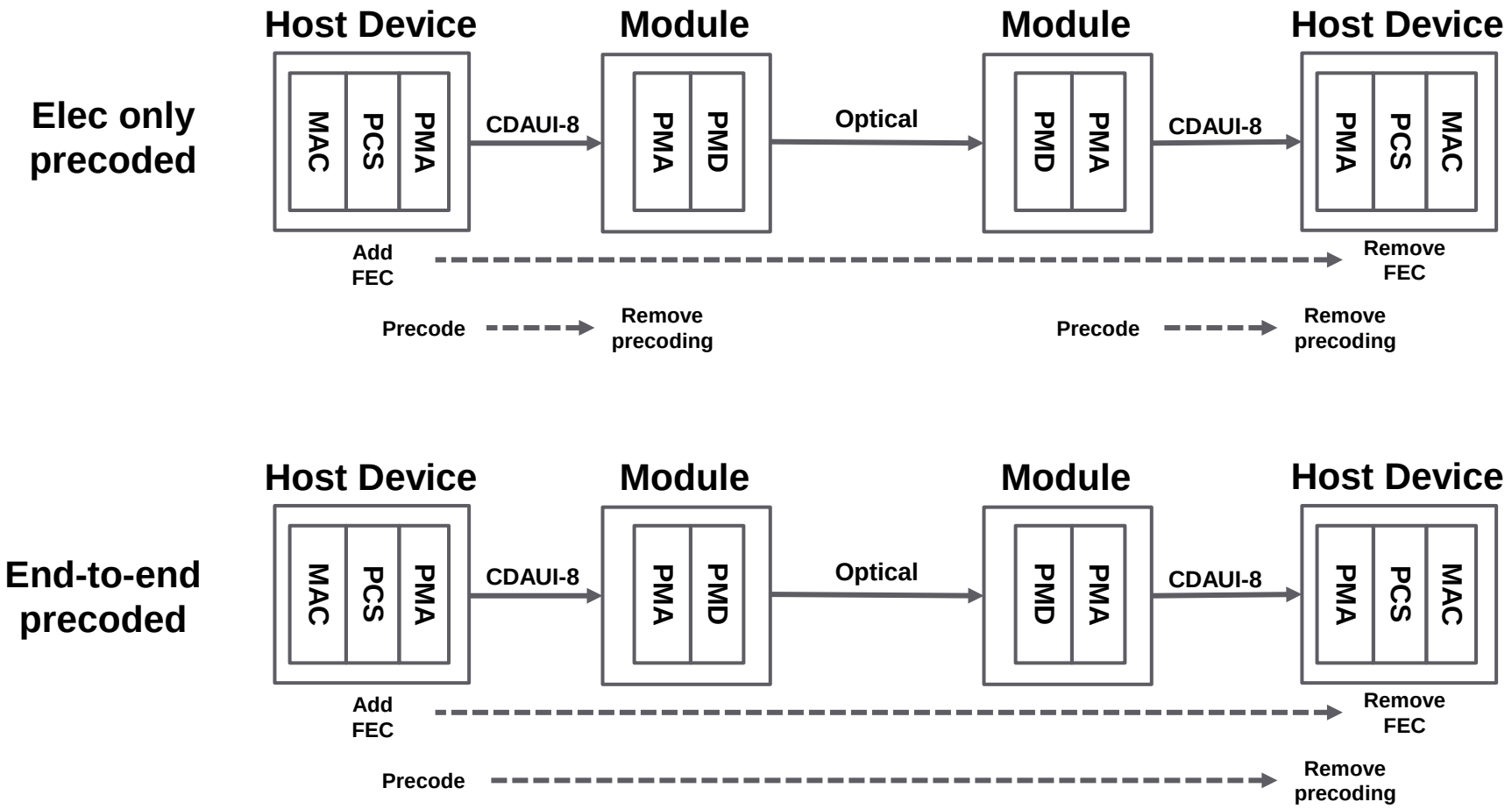
For reference, if all of the coding gain were to be used for the PAM4 link, the BERs at the slicer output and FEC input required to give FLRs equivalent to that of a BER of 1E-13 and 1E-15 are:

	At slicer output		At FEC input	
	FLR = 6.2E-11	FLR = 6.2E-13	FLR = 6.2E-11	FLR = 6.2E-13
No FEC	1E-13	1E-15	1E-13	1E-15
1:2 Same FEC, a = 0.75	1.8E-5*	3.6E-6*	1.8E-5	3.6E-6
1:2 Same FEC, a = 0.5	3.9E-5*	9E-5*	3.9E-5	9E-5
a = 0.75 misaligned	5.2E-5*	1.3E-5*	5.2E-5	1.3E-5
1:2 Same FEC precoded, a=0.75	2.3E-4*	1.3E-4*	1.1E-4	6.3E-5
1:2 Same FEC precoded, random	7E-5	4E-5	1.4E-4	8E-5
Precoded, a=0.75	2.4E-4*	1.3E-4*	1.2E-4	6.7E-5
Precoded, random	1.3E-4	7.9E-5	2.6E-4	1.6E-4
Random errors	3.2E-4	2.3E-4	3.2E-4	2.3E-4

Note – these values are the BER **including** the additional errors due to the bursts. To account for burst errors, the values marked with "*" have been multiplied by 4 when a = 0.75 and 2 when a = 0.5.

Precoded multi-part links analysed

Two different schemes for precoded links have been analysed in the next slide:



Multi-part link results

The BER of the electrical sub-links for a penalty of ~0.1 dB optical in the optical sub-link are shown in the table below.

	At slicer output for FLR = 6.2E-11			
	Electrical		Optical	
1:2 Same FEC, a = 0.75	Burst	1.4E-6*	Random	2.4E-4
1:2 Same FEC, a = 0.75	Burst	2.9E-6*	Random	2E-4
1:2 Same FEC, a = 0.5	Burst	1.6E-5*	Random	2.4E-4
a = 0.75 misaligned	Burst	5.2E-6*	Random	2.4E-4
1:2 Same FEC elec only precoded, a=0.75	Burst	5.1E-5*	Random	2.4E-4
1:2 Same FEC end-to-end precoded, a=0.75	Burst	6.9E-5*	Random	4.9E-5
Random errors	Random	8.2E-5	Random	2.4E-4

Note – these values are the BER **including** the additional errors due to the bursts. To account for burst errors, the values marked with "*" have been multiplied by 4 when a = 0.75 and 2 when a = 0.5.

Conclusion

The performance for end-to-end precoding (precode prior to electrical sub-link at transmitting end and removing the precoding only after the electrical sub-link at receiving end) is very poor for 1:2 bit interleaving. This is because each random error made in the optical sub-link turns into a pair of errored PAM4 symbols, one from each 25G PCS lane (and therefore from two different FEC symbols).

The performance for adding and removing precoding at each end of the electrical sub-links and not precoding the optical sub-link is good for a=0.75 burst probability as long as the error burst due to the DFE follows the pattern expected from a 1 symbol DFE as shown on page 5 of parthasarathy_01_0911 (error event row).

However, simply restricting the DFE parameters so as to reduce the burst probability to a=0.5 has the effect of increasing the allowable BER contributed by the electrical links to 1.6E-5 (16 x the max value for each link in the adopted baselines).

Thanks!