1 x 400G vs. 4 x 100G FEC performance further analysis

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IEEE P802.3bs Task Force, Waikoloa, July 2015

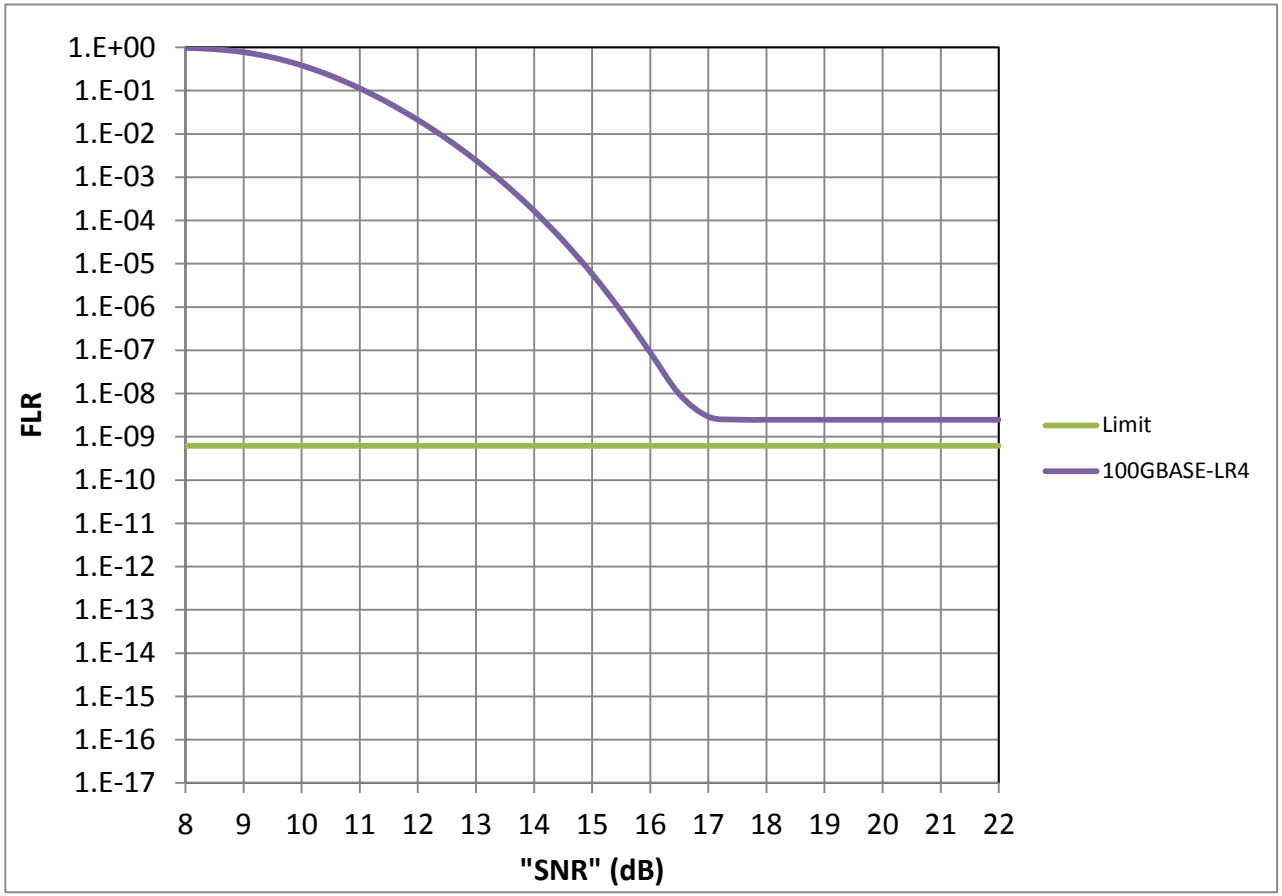
Introduction

Contributions wang_x_3bs_01_0715 and wang_t_3bs_01_0715 describe 400Gb/s Ethernet as suffering from an “error floor”.

This presentation looks at the performance of the proposed 1 x 400G FEC scheme for P802.3bs in the context of the performance of the existing 100GBASE-LR4 with CAUI-10 as defined by the P802.3ba project.

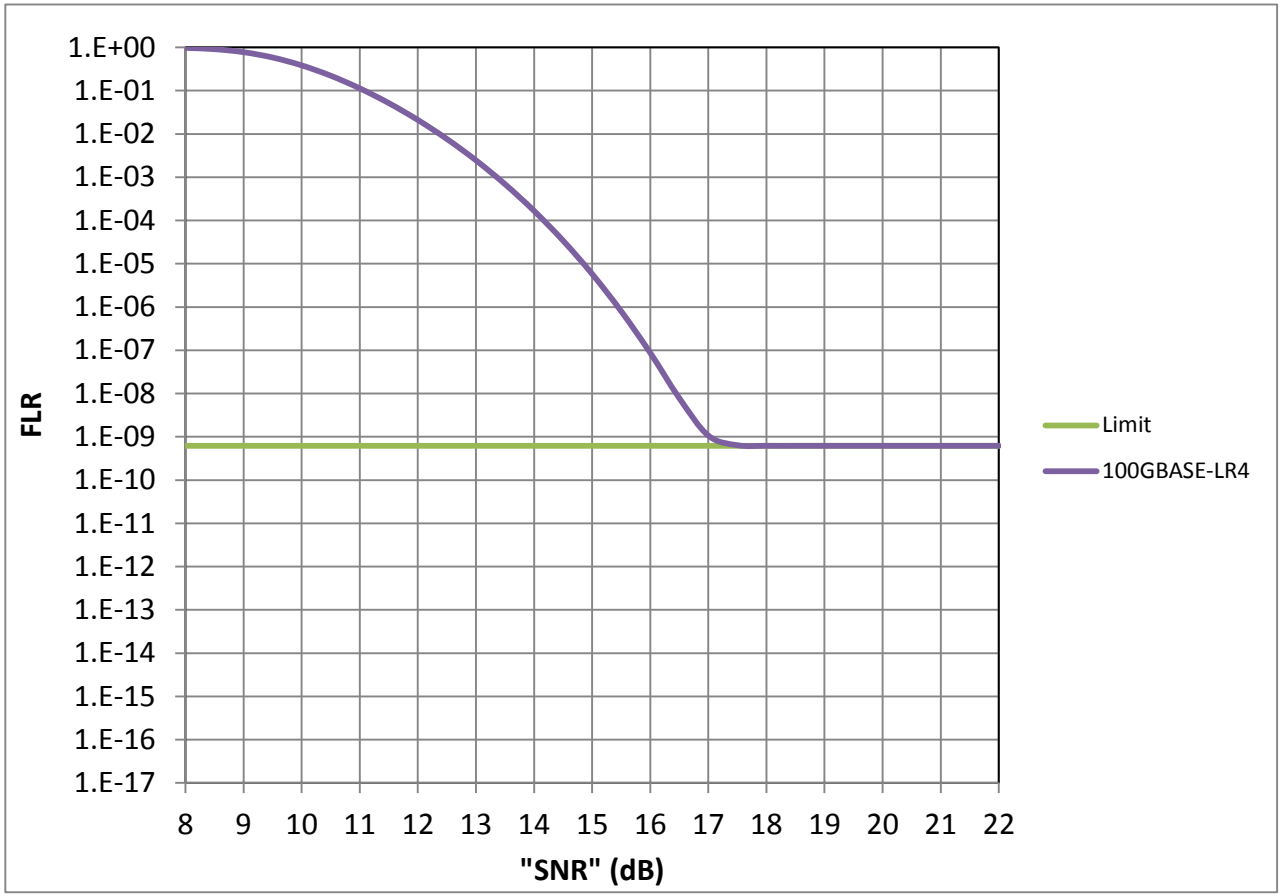
Analysis of 100GBASE-LR4 1

If we analyse the BER performance of 100GBASE-LR4 using CAUI-10 with the same methods as slide 10 of wang_x_3bs_01_0715 (assuming multiple electrical links all at their worst case BER) we get:



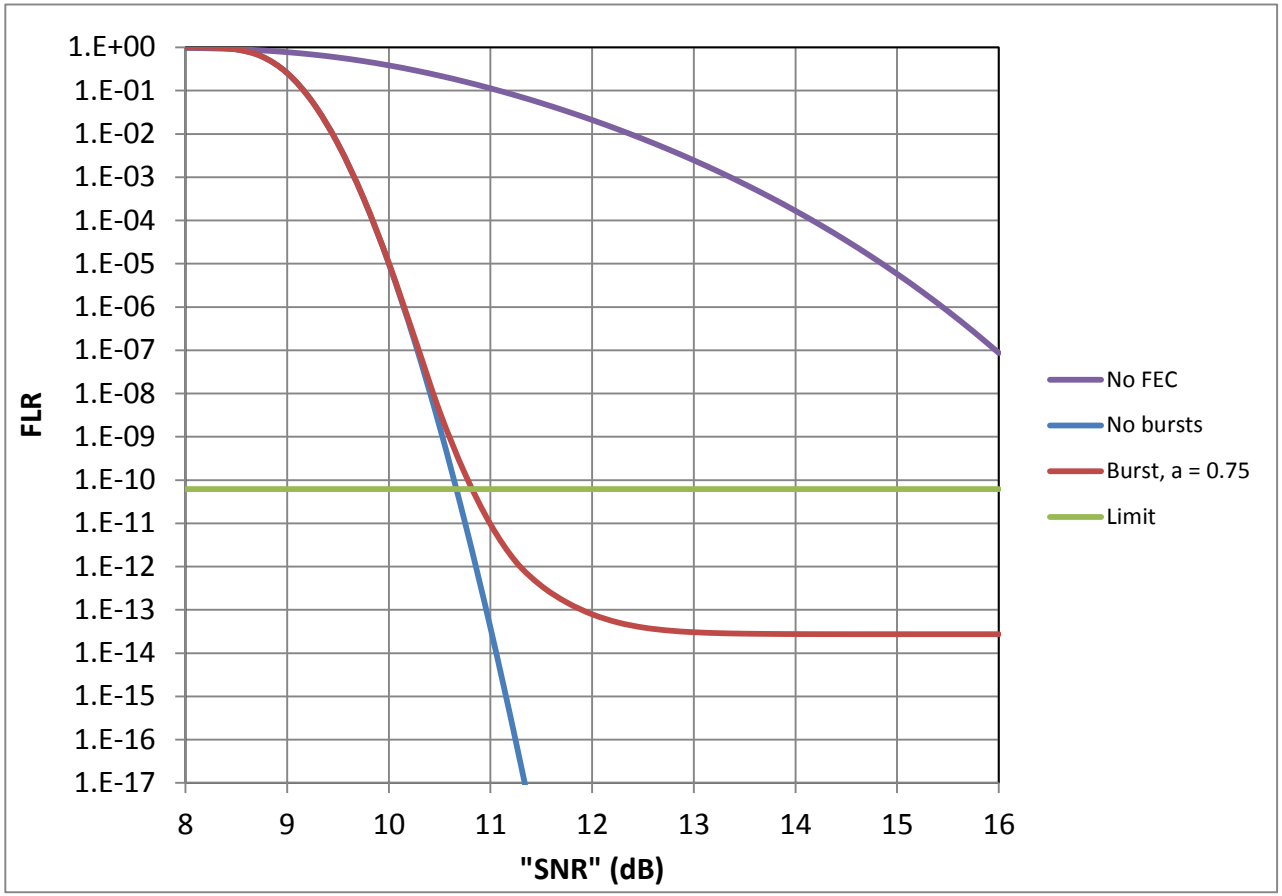
Analysis of 100GBASE-LR4 2

If we analyse the BER performance of 100GBASE-LR4 using CAUI-10 with the assumption made in P802.3ba – only one electrical link (with all of its lanes at the worst case BER) we get:



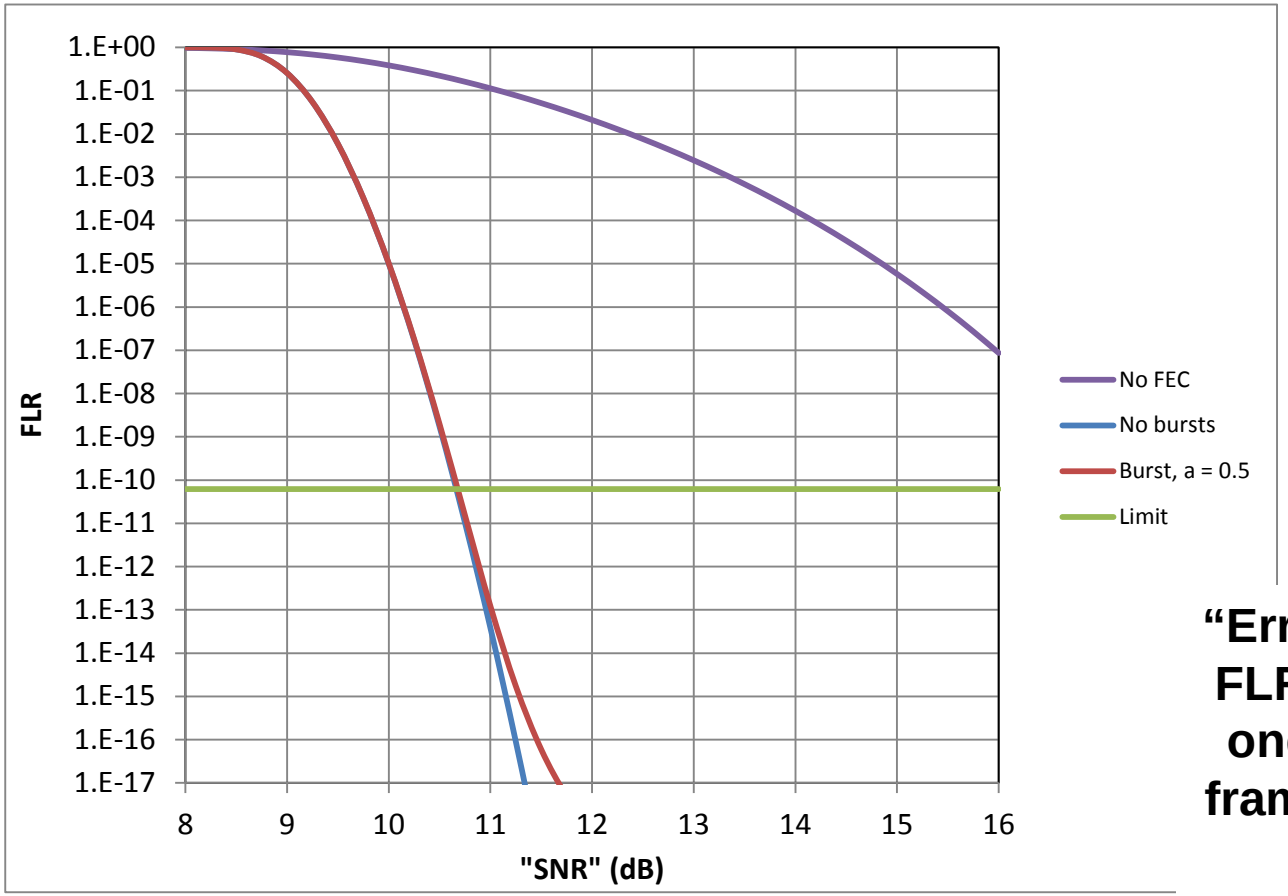
Analysis of 400GBASE-LR8 1

If we analyse the BER performance of 400GBASE-LR8 using CDAUI-8 with the assumption made in P802.3ba – only one electrical link (with all of its lanes at the worst case BER and all a = 0.75) we get:



Analysis of 400GBASE-LR8 2

If we analyse the BER performance of 400GBASE-LR8 using CDAUI-8 with the assumption that two electrical links (with all of their lanes at the worst case BER and all a = 0.5) we get:



"Error floor" at FLR = 7.3E-19 one dropped frame every 67 years

Conclusion

If we want to use “FOM” with bit muxing then we have to use a FEC architecture with 4 x 100G. This loses us 4 orders of magnitude in actual BER with random errors from a very conservative estimate in anslow_3ba_05_0715 accounting for variation in Rx sensitivity only.

We also have to ensure that two lanes from the same FEC instance are never multiplexed together. Two ways of doing this are:

- Make the chip that does simple bit muxing read the lane markers and pick lanes appropriately
- Abandon the any lane goes anywhere principle and fix the lane structure, e.g. optical lane 0 is a mux of PCS lane 0 and 4

An alternative to FOM to improve performance that does not have a penalty with random errors and does not reduce lane routing freedom would be to restrict the DFE taps such that the parameter $a < 0.5$ (see slide 6). This modest change gives an “error floor” of one lost frame every 67 years with two electrical sub-links operating with all lanes at the worst case BER and all with $a = 0.5$.

The latter solution seems a better choice.

Thanks!