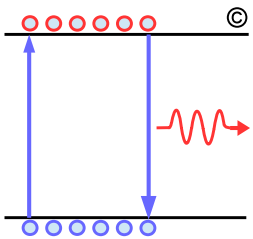


Consideration for CRU BW and Jitter Tolerance

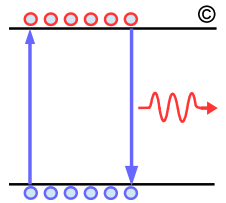
Ali Ghiasi
Ghiasi Quantum LLC

Greg Le Cheminant
Keysight

802.3bs Task Force Meeting
Waikola

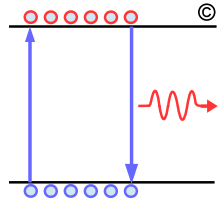
July 2015

Overview



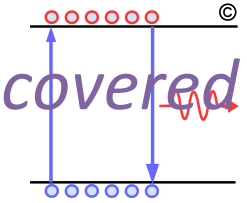
- **Consideration for CRU and CDR BW**
- **Background on jitter transfer and tolerance**
- **Review of several IEEE standard jitter filter and tolerance**
- **Fundamental issue the disconnect between transmitter and receivers**
- **Host receiver must operate with cascaded jitter**
- **Slides 4, 5, 6, and 9 are form Ghiasi – Le Cheminant addressing the same issue**
  - http://www.ieee802.org/3/bm/public/mar14/ghiasi_01_0314_optx.pdf

Consideration for CRU and CDR BW



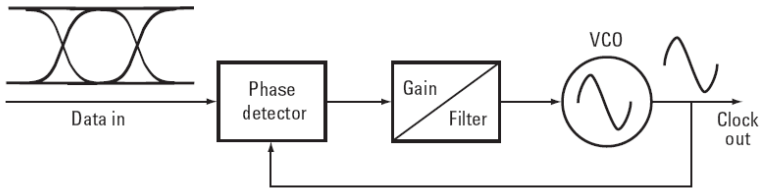
- **Consideration for the golden PLL CRU BW**
  - Oscillator phase noise
    - With most oscillator have flat phase noise> 1 MHz no benefit
  - Crosstalk
    - High frequency effects >> CRU BW
  - VCO phase noise
    - No benefit when CRU BW > 4MHz
- **Consideration for CDR BW**
  - Pattern dependent effect
    - Does not apply to 64B/66B/scrambled data with spectrum in the ~ 100 KHz
  - Power
    - Higher loop BW results in higher CDR power
  - DSP receiver
    - Timing recovery introduces latency making it challenging to meet traditional Fbaud/2578 CDR loop BW
  - Backward compatibility
    - Does an HOM port only operate at single speed with another HOM port or the port need to interoperate at lower bit rate with CAUI-4, CR4, SFI, etc?
    - An implementation requiring backward compatibility through a common data path would need 10 MHz CDR BW.

PLL concepts: PLL jitter transfer indicates how *recovered clock* (jitter out) tracks the data (jitter in)

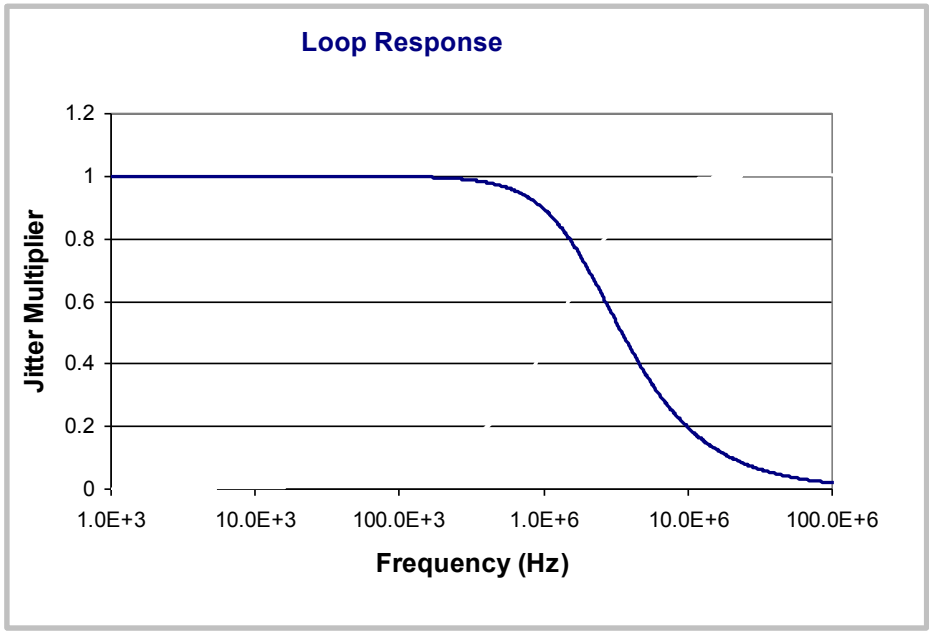


- **The response of the PLL is generally a low-pass function, sometimes referred to as the jitter transfer response or JTF**

$$\text{Closed loop gain} = \frac{\phi_{out}}{\phi_{in}} = \frac{A(s)}{1 + A(s)} = G(s) = |G(s)|e^{j\phi(s)}$$

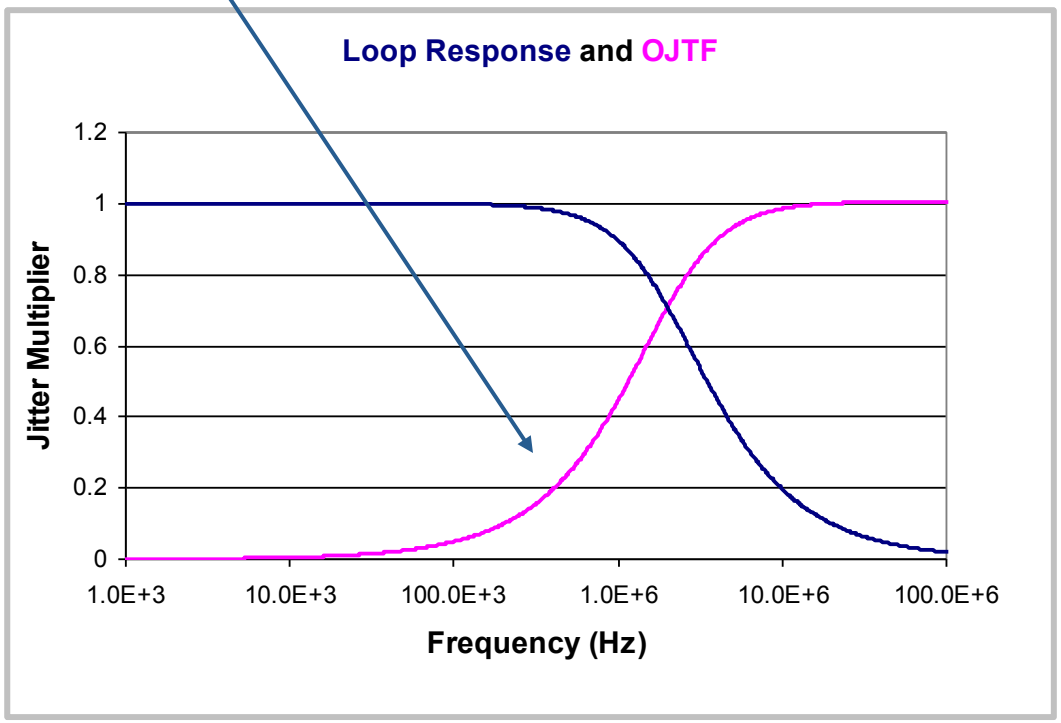


Low frequency jitter is transferred to the clock, high frequency jitter is not



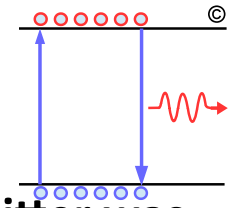
The observed jitter transfer function (OJTF, the jitter that is observed by a receiver, or on the instrument clocked/triggered by the recovered clock)

$$\mathrm{OJTF} = 1 - G(s) = 1 - \left|G(s)\right| e^{j\phi(s)}$$

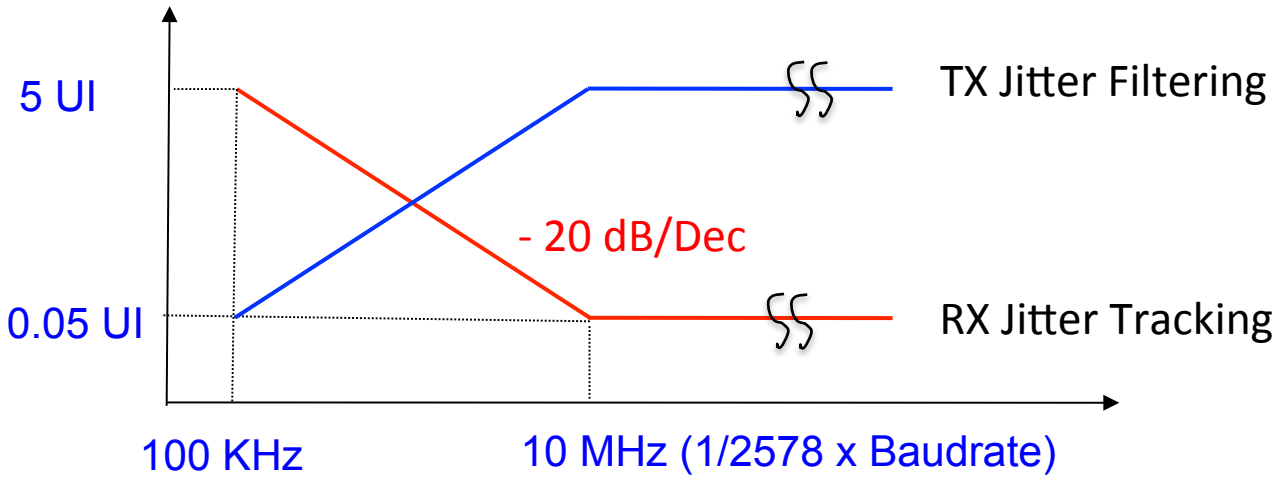


- **The observed jitter is a complement to the PLL jitter transfer response**
- **OJTF=1-JTF (Phase matters!)**
- **As the jitter on the recovered clock trigger rolls off, common mode effect is reduced**
- **As jitter frequency gets large, eventually there is no jitter on the recovered clock and all the higher frequency jitter on the data stream is observed**

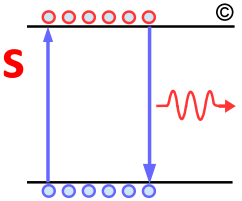
Comprehensive Jitter Methodology



- **A comprehensive methodology to test transmitters and receivers for jitter was developed during 1 GFC standardization in the FC-MJS project and has become the basis for data communications system specification**
- **This methodology was based on systems using low cost oscillators and a reduction in power supply filtering to enable low-cost high-volume applications**
  - Transmitter test assumes low frequency jitter should be tracked by a receiver, thus transmitter specs are relaxed by observing the transmitter using a reference PLL with OJTF defined as a high pass single pole filter with -20 dB/dec rolloff and -3dB corner frequency at 1/1667 Baudrate (changed to 1/2578*baudrate since 10 GbE)
  - Receiver test should complement transmitter test by verifying low frequency jitter is tolerated, example shown below is for a CRU/CDR response per CL 88.

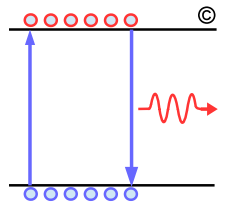


TX Jitter Filter and RX Jitter Tolerance for Several IEEE Standards



- **CL 52, 86A (40G-SR4, 100G-SR4), 83A/B (XLAUI, CAUI-10)**
  - Transmitter output measured with 4 MHz CRU (high pass jitter filter) Fabud/2578
  - Receiver is tested with worst case stress + TX credited low frequency SJ
- **CL 68 (LRM), CL 72 (10G-KR), CL 85 (40G-CR4/100G-CR10)**
  - Transmitter output measured with 4 MHz CRU (high pass jitter filter) Fbaud/2578
  - CL 68 only tested unstress at two points (75 KHz, 5 UI) and (375 KHz, 1 UI)
  - CL 72 interference test require testing receiver with 0.115 UI at Fbaud/250
  - CL 85 interference test require testing receiver with 0.115 UI at frequency > 15 MHz
- **CL 88 (100G-LR4), CL 95 (100G-SR4), CL83D/E (CAUI-4)**
  - Transmitter output measured with 10 MHz CRU (high pass jitter filter) Fbaud/2578
  - Receiver is tested with worst case stress + TX credited low frequency SJ
- **CL 92 (100G-CR4), CL 93 (100G-KR4)**
  - Transmitter output measured with 10 MHz CRU (high pass jitter filter) Fbaud/2578
  - CL 92 interference test require testing receiver with 0.115 UI at frequency > 100 MHz and unstress SJ testing at (190 KHz, 5 UI) and (940 KHz, 1 UI)
  - CL 93 tested with 35 dB ISI channel at (190 KHz, 5 UI) and (940 KHz, 1 UI)
- **CL 94 (100G-KP4)**
  - Transmitter output measured with a CRU having 20 dB/dec low frequency response, 1.6 MHz BW, and 3 dB peaking at 6 MHz, response has peaking to accommodate 2nd order loops and potential peaking as result of DSP timing recovery latency
  - Receiver is tested unstress with following SJ components (16 KHz, 5 UI) and (160 KHz, 0.5 UI), jitter tolerance actually does not reflect the intention of 2nd order CRU
- **10G-LRM and 100G-KP4 testing receivers unstress does not guarantee interoperability**
  - 10G-KR and 40G-CR4/100G-CR10 interference tolerance does have an SJ component but does not test against potential SJ allowed by the transmitter.

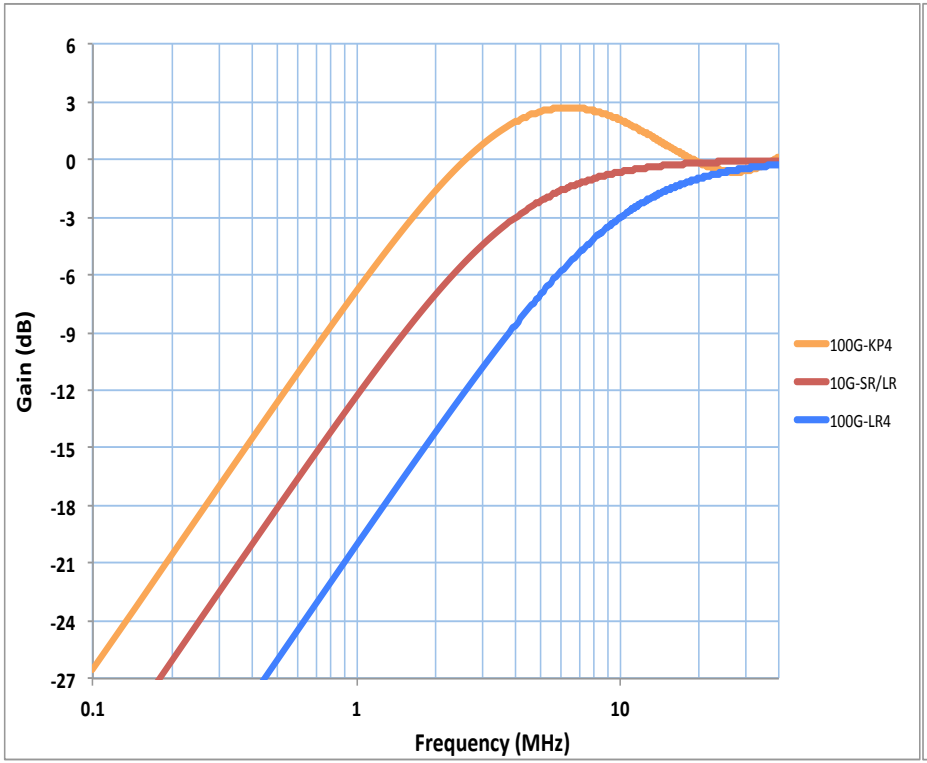
Transmitter Jitter Filter vs Receiver Jitter Tracking for Several IEEE Standards



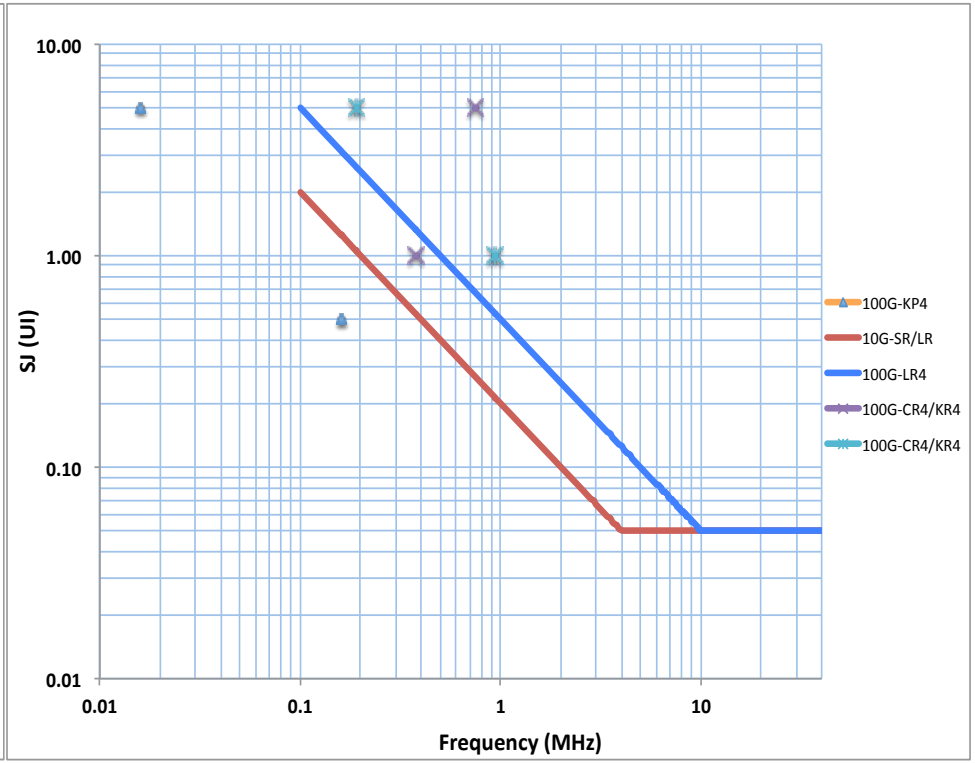
- **The receiver must track the low frequency jitter golden PLL filters for observation on the scope, only 100G-KP4 defines 2nd order response as defined by:**

$$G(f) = \frac{f}{f - j \times f_n e^{(j2\pi fT)}} \quad , \; where \; f_n = 2.12\,MHz \; and \; T = 0.0286\,\mu s$$

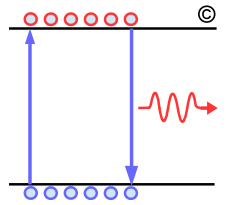
Golden PLL "TX Jitter Filter" Response



Stress Sensitivity

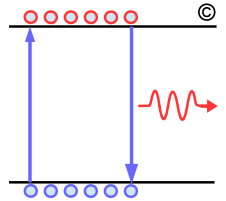


Fundamental Issue

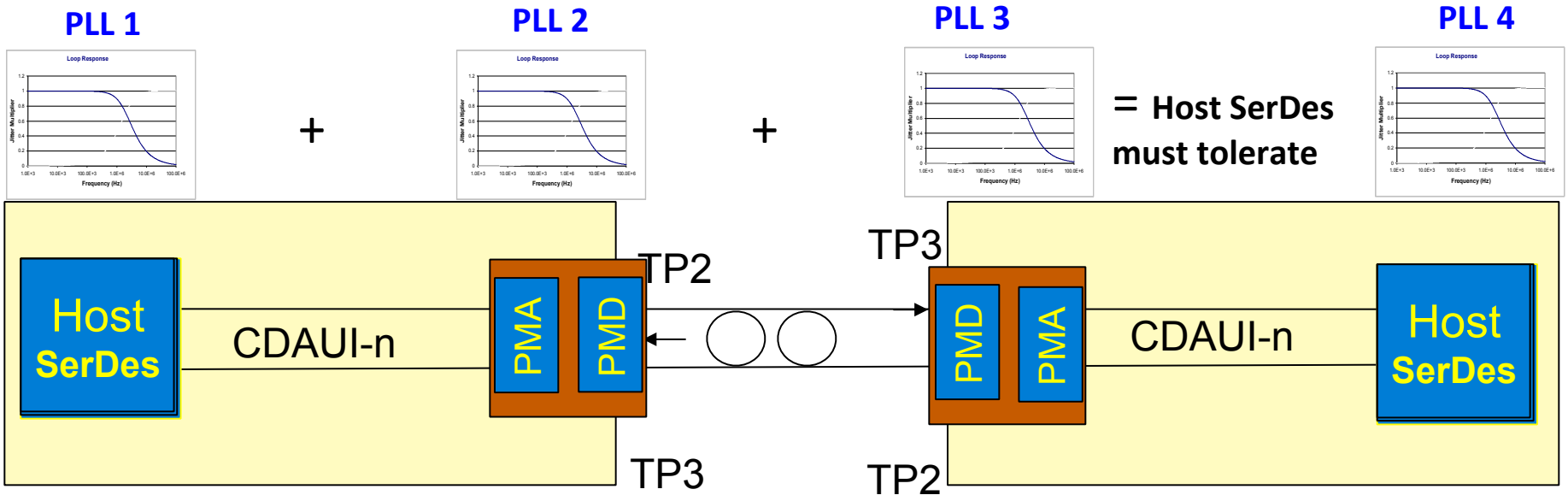


- **802.3aq (LRM) and 100G-KP4 receiver jitter tolerance introduced an inconsistent set of specifications by separating stress receiver testing and transmitter jitter tracking**
  - Transmitter jitter relief through MJS Golden PLL was maintained
    - Compliant transmitters may have low frequency jitter present, but not observed due to by the Golden PLL tracking effect
  - In IEEE the more complex receiver such as LRM and 100G-KP4 are only tested unstress at two spot frequencies as illustrated in previous slide
  - Full stress with the addition of SJ can result in broken links that is not observed with stress and SJ imposed in independent tests
  - Testing the receiver at only two discrete frequencies may not guarantee the receiver can actually tolerate transmitters with jitter tracked "masked" out by the Golden PLL
  - Transmitter tracked "masked" jitter actually propagates through the link and could break CDAUI-8 or CDAUI-16 host receiver!

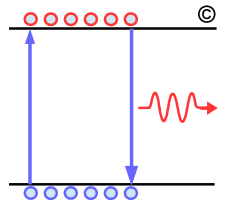
Receiver Must Tolerate all Jitter Components Propagating Down the Link



- **Unless the PMA in the module has E-FIFO the host SerDes receiver PLL 4 must tolerate low frequency jitter propagated and shaped by the PLL 1, PLL 2, and PLL 3**
  - The PMA in optical module may have a PLL BW < Fbaud/2578 if the host PLL 1 has the same BW assuming the HOM module do not interoperate with other PMDs
  - However host SerDes PLL may need to have a BW of Fbaud/2578 as the host receiver typically must support legacy PMDs.



Summary



- **Reliable link operation requires that the receiver test complements transmitter test.**
  - Any time a transmitter tested with Golden PLL which filters low frequencies jitter component that the receiver may not tolerate may result in sporadic link failures
  - Alternatively, the transmitter test could be more stringent
  - Regardless of the complexity of the receiver or the order of modulation the receiver must operate with any compliant transmitter
- **HOM receivers are more complex and their timing recovery may have higher latency which may be very difficult to support Fbaud/2578 so what are the options:**
  - Ignore the legacy support in IEEE let the market sort it but at least define set of consistent transmitter and receiver test with PLL BW << Fbaud/2578
    - Defining a PLL BW <<Fbaud/2578 will increase phase noise impacting HOM receivers
  - Define a PLL BW of 4 MHz compatible with 10G PMDs, optionally host may have a PLL BW of 10 MHz to support 100G-LR4 like PMDs
  - Define a PLL BW of 10 MHz to be fully backward compatible with existing PMDs
- **A DSP receiver with 4 or 10 MHz loop BW may have significant cost and power implication, but even worse would defining new set of standards not backward compatible or requiring PMA with E-FIFO!**