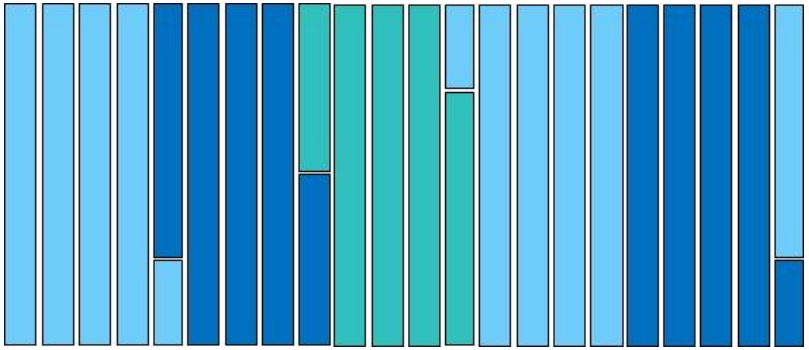
1x400GE FEC Implementation

Martin Langhammer
Altera Corporation

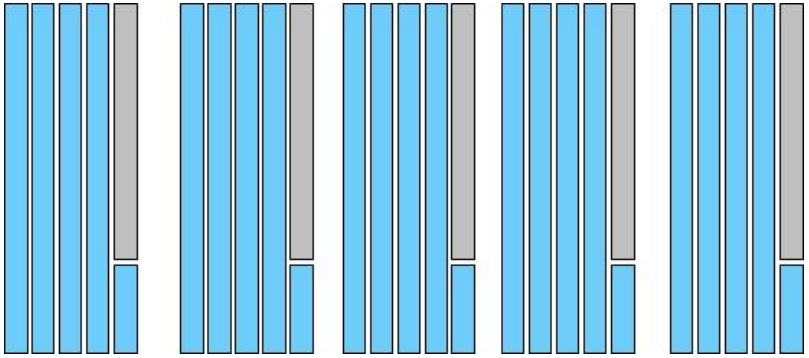
IEEE802.3bs 400GE Task Force
July, 2015

1x400GE Problem (and a fix)

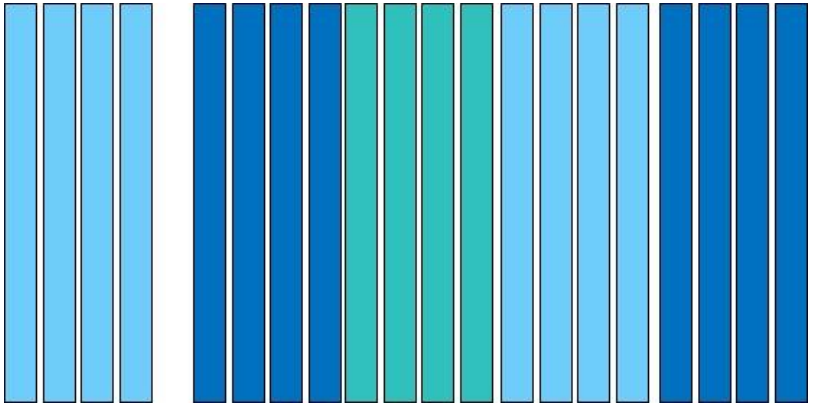
(544%128)!=0



Gearbox in Time
(run faster to have a constant input pattern)
128 width



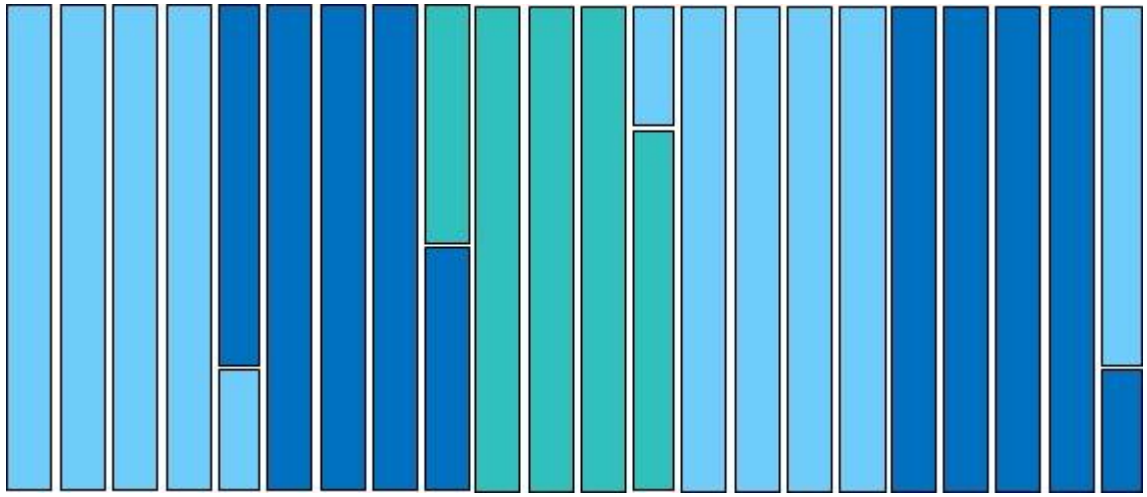
Gearbox in Width
(run faster to have a constant input pattern)
136 width



Requires Gearbox(es)
Requires Multi-clocks

Or

- Build Decoder with continuous input pattern
  - 128 symbol width
  - Direct interface to PMA and PCS
- Now working – functionally and FPGA fit



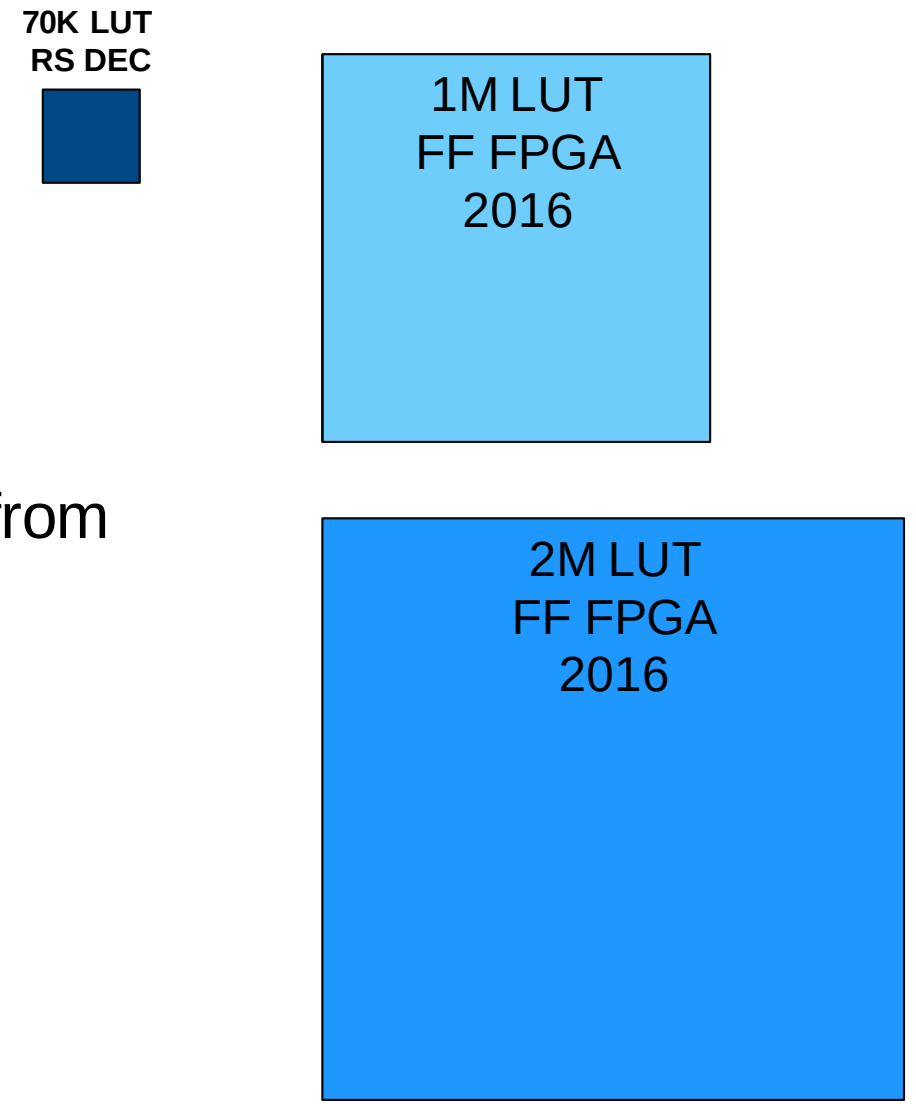
FPGA KP4 Resources (ALM ≙ 6LUT)

- 100G KP4 : 19K ALMs
  - 4x100G: 78K ALMs
  - Improved from November 2014 results
- 400G KP4 (4 x 136 symbols): 70K ALM
- 400G KP4 (128 symbol continuous): 70K ALM
- 1x400G continuous throughput same size as simple input styles
  - More complex algorithm and logic
  - Offset by slightly smaller datapath
- 1x400G slightly smaller than 4x100G

FPGA Use Considerations

- FPGA system implications
  - Area of 1x400G smaller than 4x100G
  - But 4x100G has a more decomposable routing congestion
    - Easier to fit automatically, possibly lower speed grade device
      - Time and cost consideration
  - Probably not significant reason, especially consideration likely production device technology
- Routing not so much a problem inside FEC core
  - Most busses or bus groups smaller than symbol datapath
  - Bussing can be decomposed inside FEC core
  - Bigger issue moving data to/from FEC
  - May indicate similar system concern for any FEC approach (1x400G or 4x100G)

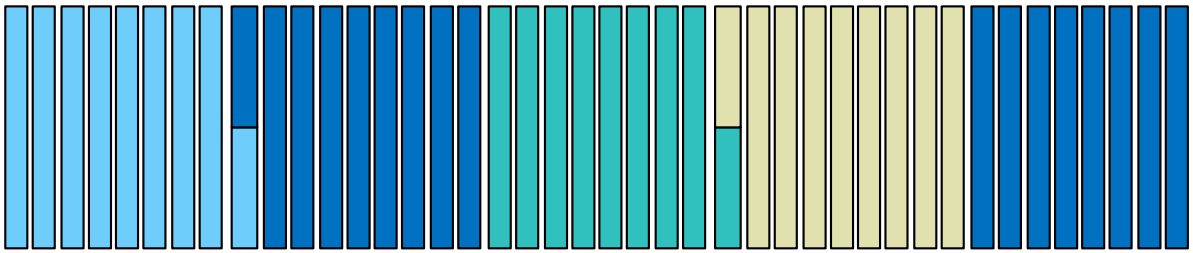
FPGA Resource Ratios



- 1x400G KP4 decoder fraction of likely target FPGAs
- Similar area roadmap from all major FPGA manufacturers

1x400GE FEC ASIC

- ASIC continuous throughput simpler pattern than FPGA continuous throughput
  - Largely because of 2x clock rate
- Simpler design
  - Simpler control structure
  - Narrower datapaths
- Designed and Implemented
  - Shown in breakout presentation



Other

- Does not require additional logic
  - No duplicated engines
    - Although this is one way of implementing these input patterns
      - Double syndrome method will add 10%-20% decoder area
      - Still not a material consideration
- No architectural difference between ASIC and FPGA approach
  - Same gate complexity
  - FPGA has more algorithmic and control complexity
    - ¼ cycle vs. ½ cycle increment
- Other input patterns can be accomodated
  - Moving to 96 symbol datapaths for future FPGAs

Conclusions

- 1x400G KP4 FEC can be made integration friendly
  - Direct connect interface with a single clock domain
- 400G FEC options relatively constant area
- FPGA fitting may be more difficult at 1x400G
  - But perhaps not
- Does not appear to be any material considerations between 1x400G and 4x100G FEC implementations
- We can choose FEC on what is best for standard moving forward

Thank You