FEC Architecture and Breakout

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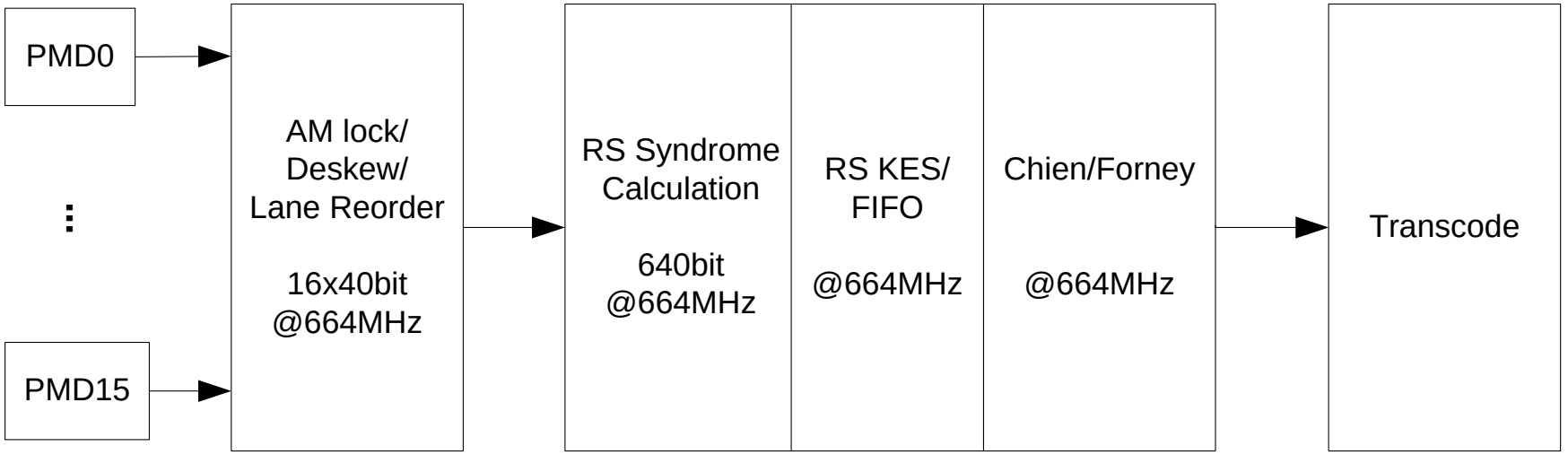
Outline

- FEC Architecture
  - 1x400G FEC
    - Design for half-cycle frames
  - 2x200G FEC
  - 4x100G FEC
- Breakout
  - Logic sharing
  - Time sharing
- Complexity and latency

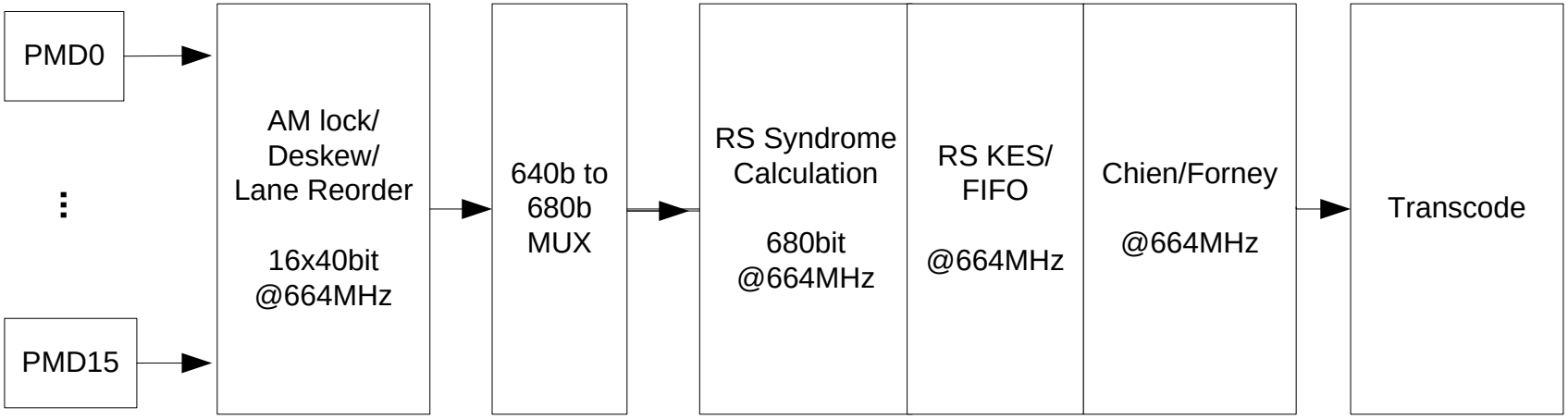
1x400G FEC: 640 bit buswidth



Block diagram for 16x25G PMD

- Easy clock scheme. Clean data path MUX for 4x100G, 8x50G, and 16x25G PMD.
- Frame latency is 8.5 cycles. Syndrome calculator: pipelined architecture with half-cycle engines to avoid external gearboxes.
- FEC decoder latency: 8+1=9 cycles for syndrome calculation, 30 cycles for KES, 8 cycles for Chien search.
- Encoder: extra data MUX or half-cycle engines for the half-cycle frames, the area is roughly 4.5x of 100G encoder.

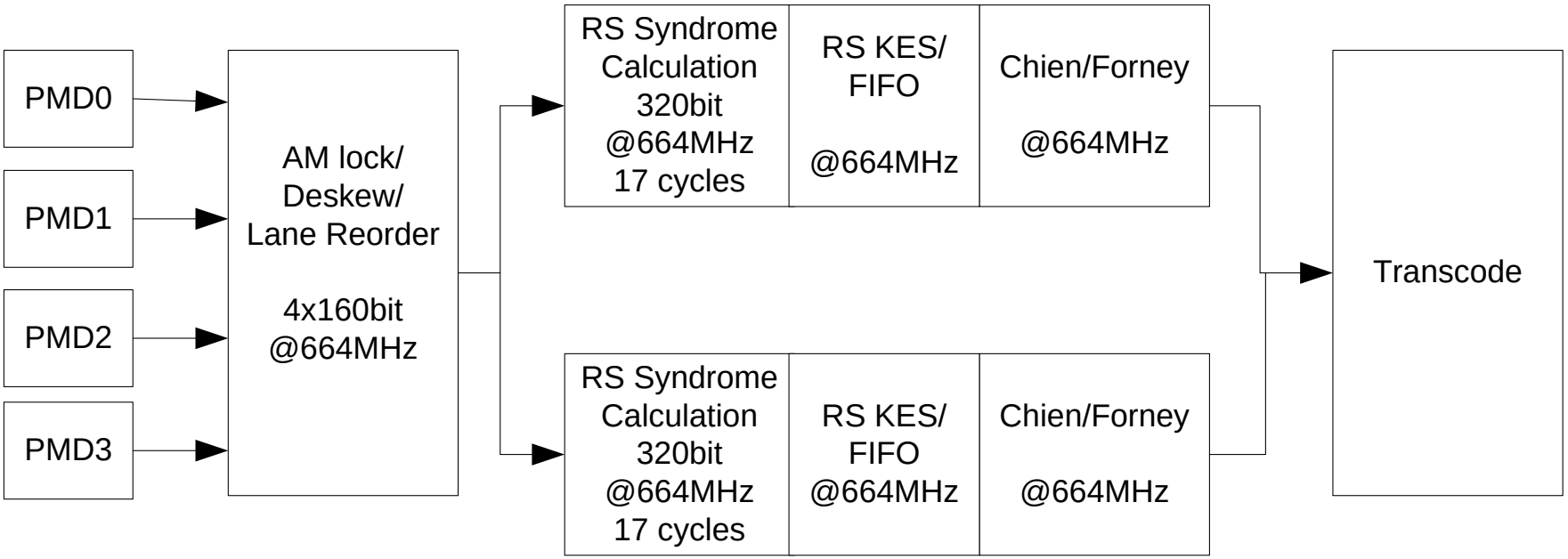
1x400G FEC: 680 bit buswidth



Block diagram for 16x25G PMD

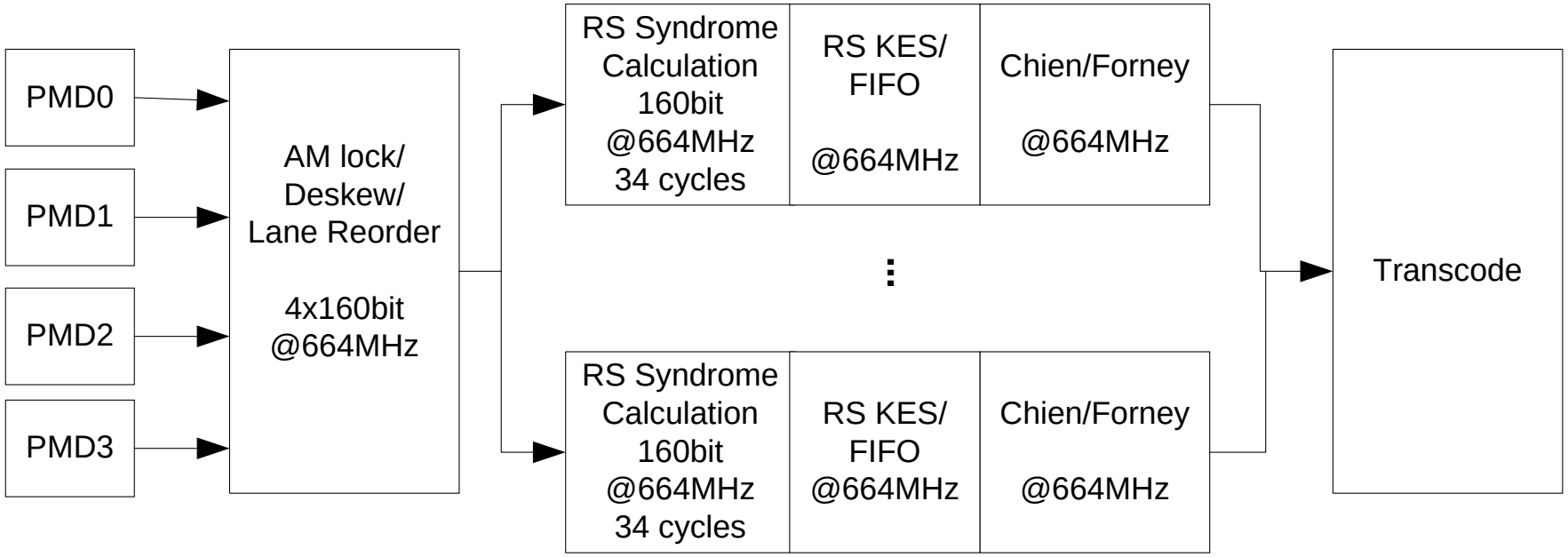
- RS frame can be received in 8 (5440/680) cycles, simple syndrome calculator.
- Lane alignment block has 640bit buswidth to avoid the half cycle issue (wang_z_3bs_01_0515.pdf). If this buswidth is 680b:
  - For 8x50G PMD, AM buswidth is 85bit. One extra cycle is needed to merge lanes as 85 is not a multiple of RS symbol size.
  - For 16x25G PMD, lane alignment logic needs to deal with 42.5bit per cycle and is complicated.
- A 640b to 680b MUX is needed.
- Latency: 1 cycle for 640b/680b MUX, 8 cycles for syndrome calculation, 30 cycles for KES, 8 cycles for Chien search.

2x200G FEC



- Easy clock scheme. Clean data path MUX to support 4x100G, 8x50G, and 16x25G.
- Frame latency is 5440/320=17 cycles. No half clock cycle issue.
- Latency: 17 cycles for syndrome calculation, 30 cycles for KES, and 8 cycles for CS.

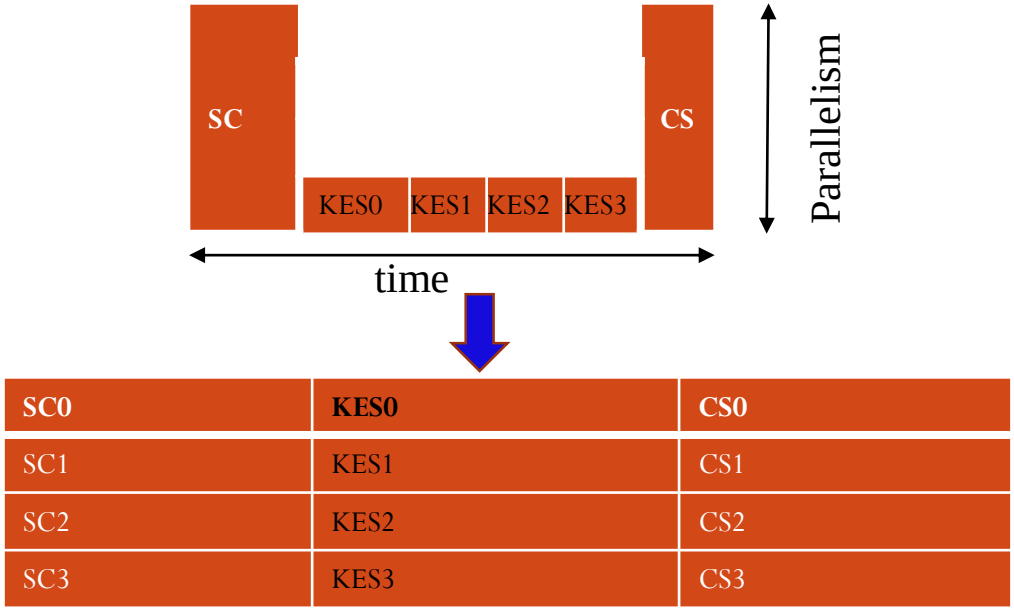
4x100G FEC



- Easy clock scheme. Clean data path MUX to support 4x100G, 8x50G, and 16x25G.
- Frame latency is 5440/160=34 cycles.
- Latency: 34 cycles for syndrome calculation, 30 cycles for KES, and 8 cycles for CS.

Breakout – logic sharing

- 4x100G KP4 breakout:
  - 1x400G and 2x200G FEC: logic sharing decoder data path
  - 4x100G FEC: natural
- 4x100G KR4 breakout:
  - 1x400G and 2x200G FEC: logic sharing decoder data path
  - 4x100G FEC: same as 802.3bj KP4/KR4 combined FEC.

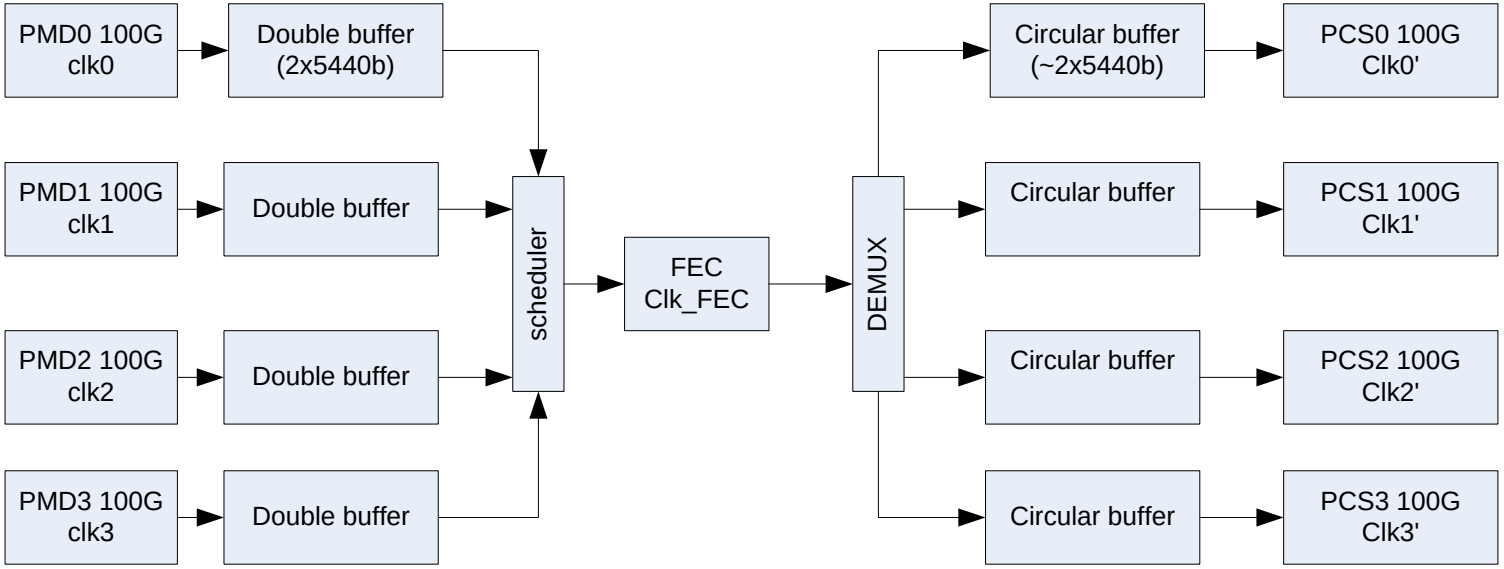


Breakout example:1x400G FEC to 4x100G KP4 FEC

Breakout - time sharing

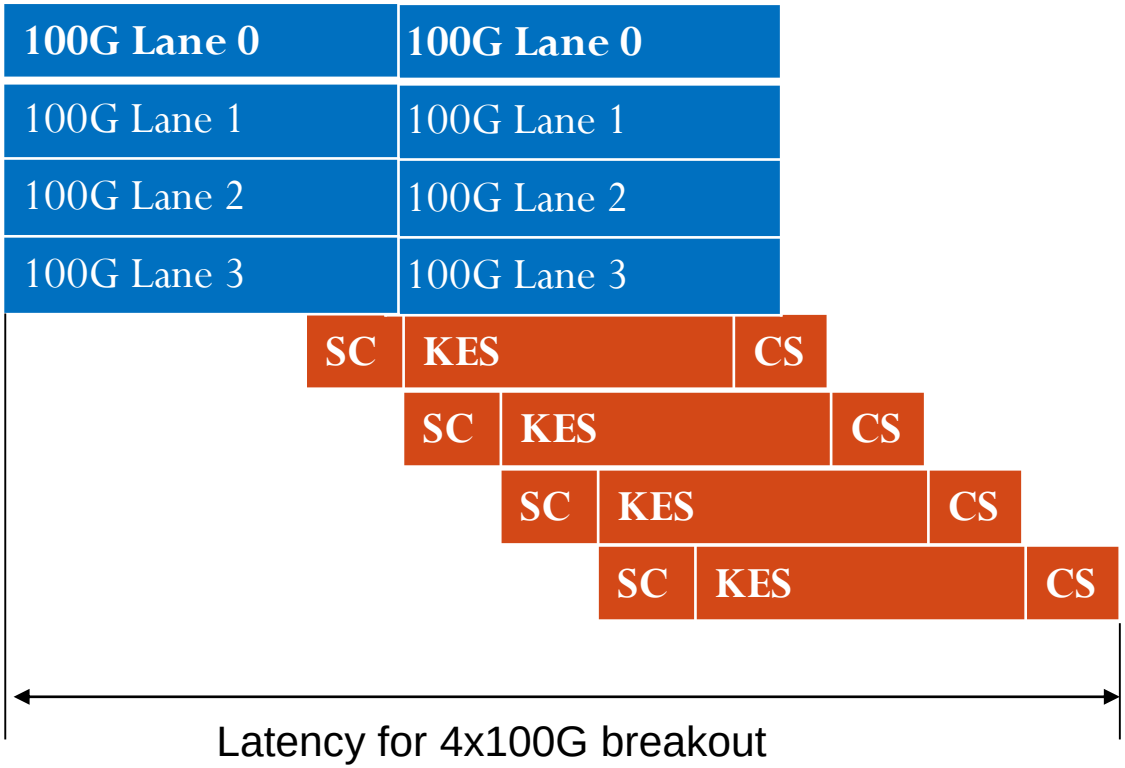
- Time share the same decoder
- For a basic time sharing decoder, latency is roughly:

  frame latency+ (n-1)Tp+KES+CS+Tb cycles, TP and Tb are the latency of the syndrome calculator and the second buffer.



Breakout: Time Sharing

- Latency illustration: 1x400G FEC



Complexity: w/o breakout

- CS latency is targeted to 8 cycles for all FECs.
- Relative complexity is listed for all major blocks.
- 1x400G FEC uses 640b bus width. The overhead is to deal with half-cycle frames.
- No big difference in hardware cost. 2x200G has the smallest area.

Breakout	Encoder	Syndrome	KES	CS	Forney
1x400G FEC	4.5x	4.4x	4x	1	4.4x
2x200G FEC	4x	4x	4x	2	4x
4x100G FEC	4x	4x	4x	4	4x

KP4 Breakout Summary

- **Decoder Latency**:

Breakout	1x400G KP4	2x200G KP4	4x100G KP4
1x400G FEC Latency(ns)	**72**	96(L), 135(T)	146ns (L), 197ns (T)
2x200G FEC Latency (ns)	84	84	122(L), 186(T)
4x100G FEC Latency (ns)	110	110	**110**

  - (L) and (T) mean by logic or time sharing.
  - Latency includes error marking.
  - About 3 extra cycles may be needed for 1x400G and 2x200G FEC to close timing.
  - Logic sharing latency difference is from error marking. For 4x100G breakout, 4x CS engines are needed for 1x400G and 2x200G FEC to achieve 110ns (+~5ns for timing closure) latency.

- **Encoder Latency**: ~3ns for all cases.
- **Complexity**:
  - Decoder by logic sharing:
    - Data paths are shared, roughly 10% design overhead.
    - More logic needed for 8x50G or 16x25G breakout for all FECs.
  - Decoder by time sharing: control logic + data mux + multiple 5Kb memories.
  - Encoder: extra engines.

KR4 Breakout Summary

- Decoder Latency by logic sharing:

Breakout	1x400G KP4	2x200G KR4	4x100G KR4
1x400G FEC Latency(ns)	72	72	120
2x200G FEC Latency (ns)	84	60	96
4x100G FEC Latency (ns)	110	84	84

- Latency includes error marking.
- About 3 extra cycles may be needed for 1x400G and 2x200G FEC to close timing.
- The number of CS engines are on slide 8.
- For 4x100G breakout, extra CS engines can be added for 1x400G and 2x200G FEC to achieve 84ns (+~5ns for timing closure) latency.

Conclusions

- Discussed designs for 1x400G, 2x200G, and 4x100G FEC, including
  - possible implementations for 1x400G FEC “half-cycle” frame length.
  - latency and complexity analysis.

- Breakout can be achieved by logic or time sharing.