Summary of 400GbE FEC Architecture

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Introduction

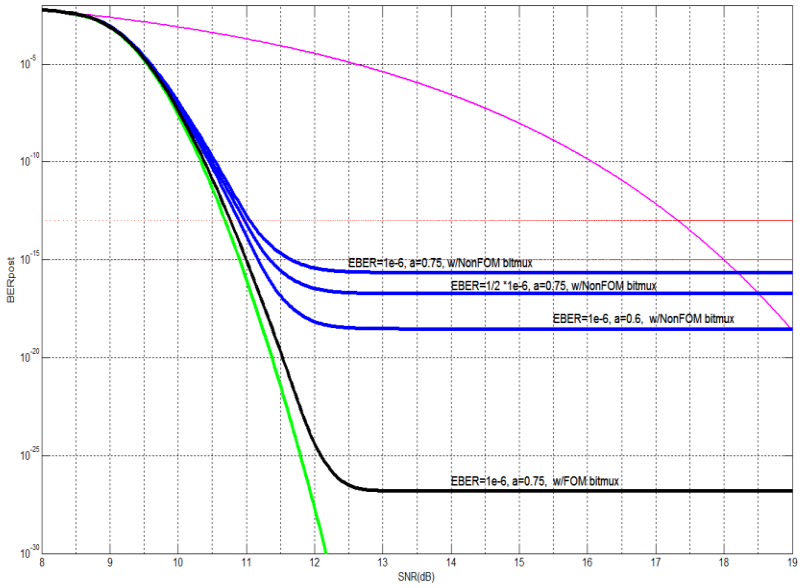
- This presentation summarize the investigation on 400GbE FEC architecture for 1X400Gbps versus 4X100Gbps KP4 FEC after Pittsburgh Meeting and logic ad hoc discussions.
- The following items are considered for comparing these two FEC architectures:
  - FEC Performance
  - Hardware complexity
  - Latency
  - Breakout

Assumption

- Underlying assumptions
  - ASIC implementation @664MHz
  - Latency estimation based on Slide #6 of consensus contribution "*wang_x_3bs_01a_0115*"
  - 640bit data path solution with half cycle process
  - No 680bit data path solution due to CDC(clock domain) issue and additional significant hardware by Gearbox as in slides #5&6 of "*wangt_01_0615_logic*"
  - 1X400G FEC breakout into 4X100G FEC, logic sharing proposal from "*langhammer_01_0615_logic*" and "*sun_3bs_01_0715*"
  - Time division multiplexing not considered due to large latency introduced by additional buffer
  - Bit Mux only for FEC performance evaluation

FEC Performance with 1x400G Bit Mux

- 1X400G FEC can support simple bit mux (NON-FOM) if the channel and/or receiver are constrained
- "Adequate" performance for electrical BER ~1E-6 and optical BER ~2E-4 as in "*anslow_3bs_03_0515*", with error floor
  - Even if one assumes no burst error exists on optical link, CDAUI-8 portion of link with error floor @~1E-16 for NON-FOM bit mux may limit the system performance due to error propagation from DFE in Chip-Chip interface.
- Diluting errors from lane with poor BER impacts multiple lanes with good BER:
  - Assumes good lanes are able to adapt to have better BER than spec.
  - Benefits diminishing for 50G/100G lanes.
  - Not helpful to lower error floor.



FEC Performance with 4x100G Bit Mux

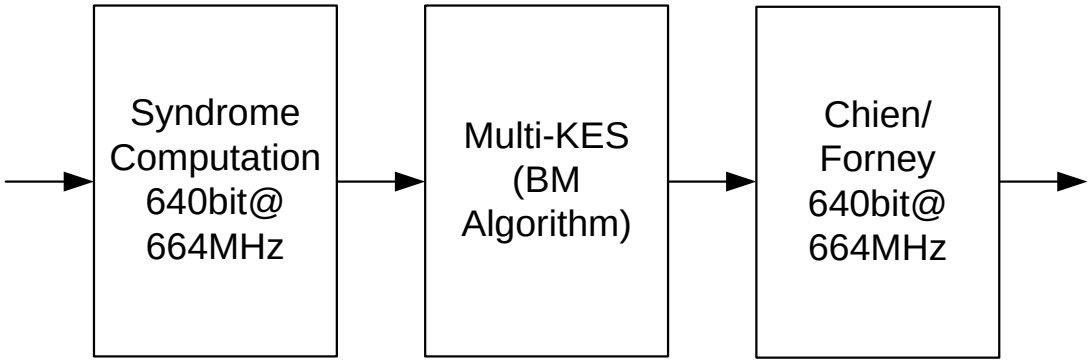
- 4X100G FEC support:
  - Simple bit mux (NON-FOM) among FEC symbol lanes from one 100G FEC
  - Orthogonal bit mux (FOM) among FEC symbol lanes from multiple 100G FEC when DFE/MLSE is needed in optical/cable PMDs.

	BERpost = 1E-13 with KP4 FEC			
	Electrical Link*		Optical Link	
Non-FOM Bit mux	Burst	4.00E-06	Random	2.00E-04
FOM Bit mux	Burst	8.00E-05	Random	2.00E-04
FOM Bit mux	Burst	1.60E-05	Random	3.00E-04

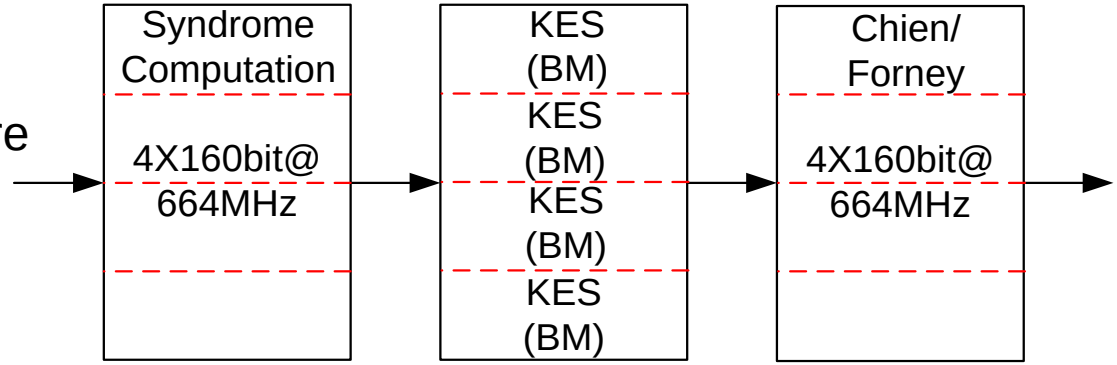
*BER requirement on multiple electrical links from PCS FEC to PCS FEC

Structure and Hardware Complexity

- 1X400G FEC Architecture (Decoder)



- 4X100G FEC Architecture (Decoder)



- 1X400G FEC Architecture timing has more challenge than 4X100G FEC from slides #8 of "*langhammer_01_0615_logic*" from FPGA perspective
- Encoder of 1X400G FEC is harder as slides #4 of "*wangt_01_0615_logic*"

Breakout to 4X100G KP4 FEC

- Assuming similar size of 1X400G and 4X100G FEC as slides #8 of "*langhammer_01_0615_logic*" and "*sun_3bs_01_0715*"
- For latency from "*sun_3bs_01_0715*":

	1X400GE FEC	Breakout 4X100GE KP4 FEC
1X400G FEC Architecture	72ns	146ns
4X100G FEC Architecture	110ns	110ns

- For hardware complexity:
  - Additional roughly ~10% logic increased as in "*sun_3bs_01_0715*"
  - Encode need additional engine as slides #11 of "*sun_3bs_01_0715*"
  - Breakout will further increase timing challenge as in slides #8 of "*langhammer_02_0615_logic*"

Breakout to 4X100G KR4 FEC

- Assuming KR4 FEC is a subset of KP4 FEC
- For latency from "*sun_3bs_01_0715*":

	1X400GE FEC	Breakout 4X100GE KP4 FEC	Breakout 4X100GE KR4 FEC
1X400G FEC Architecture	72ns	146ns	120ns
4X100G FEC Architecture	110ns	110ns	84ns

- 4x100G FEC offers competitive latency with additional flexibility.

Summary

- From Hardware complexity perspective, 1X400G FEC has timing challenge as 4X100G FEC is mature technology
- From Latency perspective, 1X400G FEC has ~38ns advantage than 4X100G FEC
- From Breakout perspective, 1X400G FEC has no more significant latency advantage with additional hardware and impact on timing closure
- From FEC performance perspective, 1X400G FEC with bit muxing will limit current and future architecture by limiting DFE and MLSE due to potential burst error
- Suggestion: 4X100G FEC in 400GbE project

Thank you