Further Clarification of FEC Performance over PAM4 links with Bit-multiplexing

Xinyuan Wang-Huawei

Ali Ghiasi- Ghiasi Quantum

Tongtong Wang-Huawei

Background and Introduction

- KP4 FEC performance is influenced by PMA multiplexing scheme, error model and BER in physical link. The following contributions are presented in Pittsburgh:
  - FEC Performance over PAM4 links with Bit-multiplexing
    http://www.ieee802.org/3/bs/public/15_05/wang_t_3bs_01_0515.pdf
  - FEC performance with PAM4 on multi-part links
    http://www.ieee802.org/3/bs/public/15_05/anslow_3bs_03_0515.pdf
- In this contribution, following considerations are investigated to address FEC performance in 400GbE
  - Burst error in optical links
  - Performance on “Bursty+Bursty” link
  - Error floor Issue
  - Influence from worst FEC Lanes
- 1X400G FEC with Non-FOM bit mux will limit current and all future implementations with DFE tap >= 2 and/or MLSE!

Potential Source of Burst Error

- Infrequent pattern dependent event.
- DC blocking caps: low frequency cut off coupled with data wonder.
- Long data transition charging effect coupled with non-linear response of O/E devices.
- VCSEL slow turn off (see page 9) has similar error floor as seen commonly in 802.3bs SMF contributions as result of top 3 effects.
  - http://www.ieee802.org/3/100GNGOPTX/public/mar12/plenary/ghiasi_02_0312_NG100GOPTX.pdf

DC Block Penalty with PRBS31

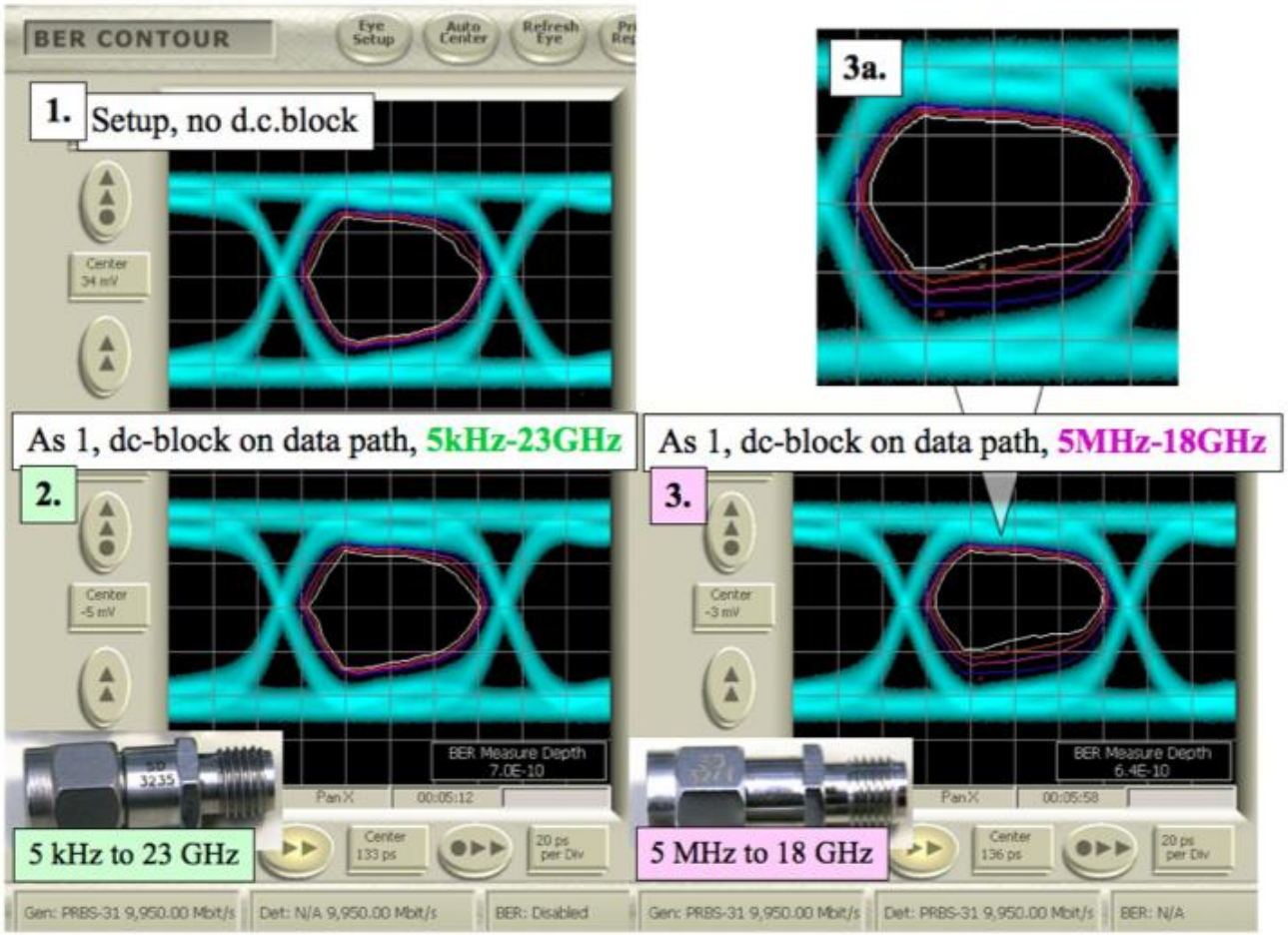


Figure 3. Passing 9.95 Gb/s data using a PRBS-31 pattern. (1) shows the signal after passing through the measurement setup but d.c. coupled; (2) has the better of the two d.c. blocks in place, (3) has a 5 MHz lower frequency cutoff and shows significant eye degradation.

http://www.tek.com/dl/65W_26043_0_Letter.pdf

Non Linear Response Coupled with Long Data Patterns

- Long tail associated with PRBS31 like pattern coupled with non-linear response of EA can result in infrequent degradation period which may result in an error burst.

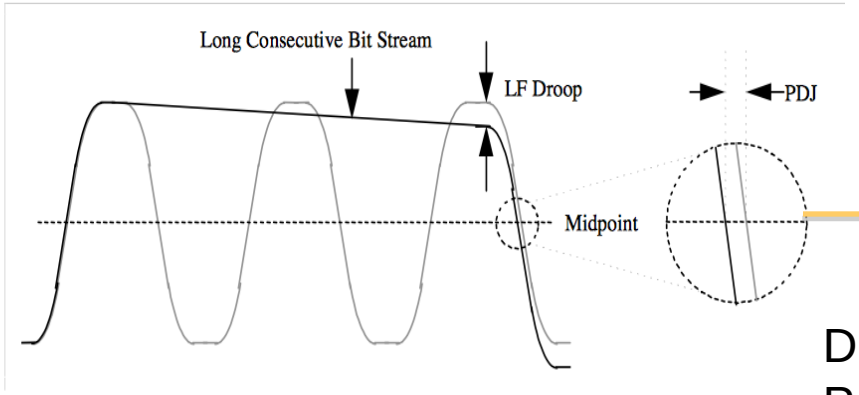


Figure 1. Low-frequency pattern-dependent jitter caused by AC-coupling

http://pdfserv.maximintegrated.com/en/an/AN292.pdf

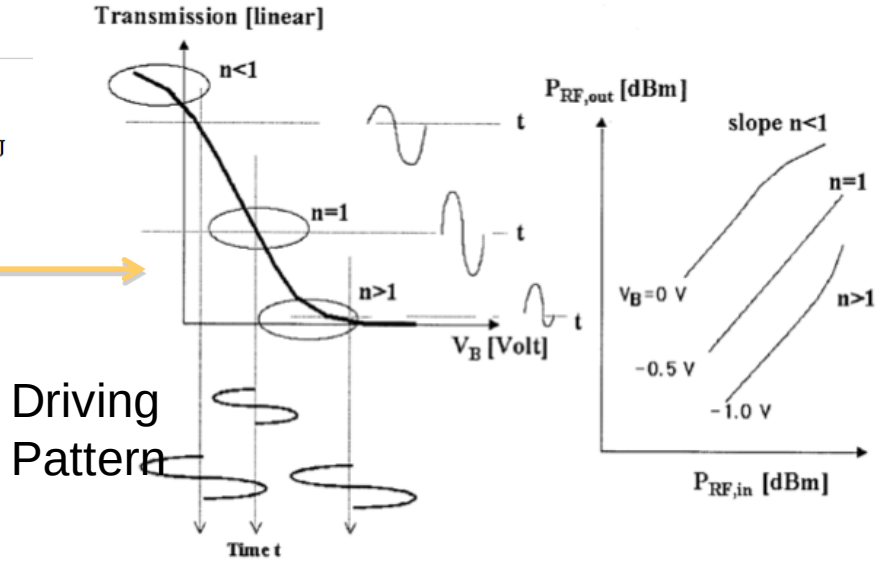


Fig. 1. Schematic plot of the relation between RF input and output powers for three different bias voltages in the TWEAM.

http://optoelectronics.ece.ucsb.edu/sites/default/files/publications/shim04ptl.pdf

Don’t Assume Optical Receiver Won’t Have DFE or MLSE !

- Traditional NRZ optical link operates with open eye with simple slicer CRU where noise is dominated
- The 50G and 100G/lane PAM4 links may have significant transmitter and receiver impairments where simple CRU slicer is no longer viable.
  - A CTLE receiver where high frequency is emphasized has limited benefit plus noise enhancement penalty
  - An FFE receiver can better equalize an optical link including fiber dispersion but FFE also has noise enhancement penalty
  - A DFE receiver is very effective to equalize bandwidth limited component of an optical link without noise enhancement at expense of burst error
- Implementing long DFE with PAM4 signaling is complex but we shouldn't rule out a short 2-3 taps DFE and an MLSE and assume optical links have absolutely no burst error!

Burst Error From DFE/MLSE Usage of PAM4 Optical link

- In "wang_t_3bs_01a_0315":
  - Chris Cole, Ilya Lyubomirsky, Ali Ghiasi, Vivek Telang, "Higher-Order Modulation for Client Optics", IEEE Communications Magazine, March 2013
    - Figure 2 shows an RX DSP-based adaptive equalizer with feed-forward equalizer (FFE) and decision feedback equalizer (DFE) blocks.
    - An FFE is characterized by the number of taps and their spacing; either T-spaced (symbol rate) or T/2-spaced (fractional). An FFE approximates the channel matched filter response and equalizes the precursor portion of the ISI.
    - A DFE is characterized by the number of taps and cancels the post-cursor portion of the ISI.

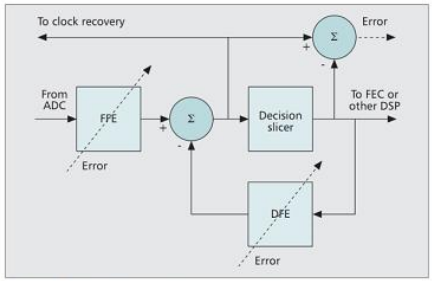
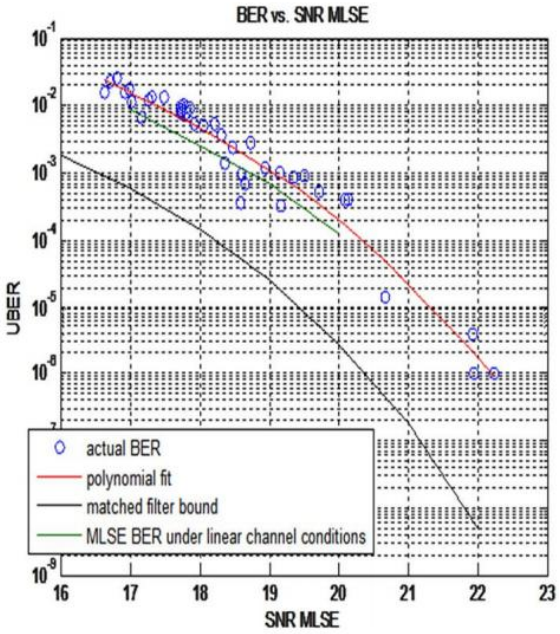


Figure 2. *RX DSP adaptive equalizer block diagram.*

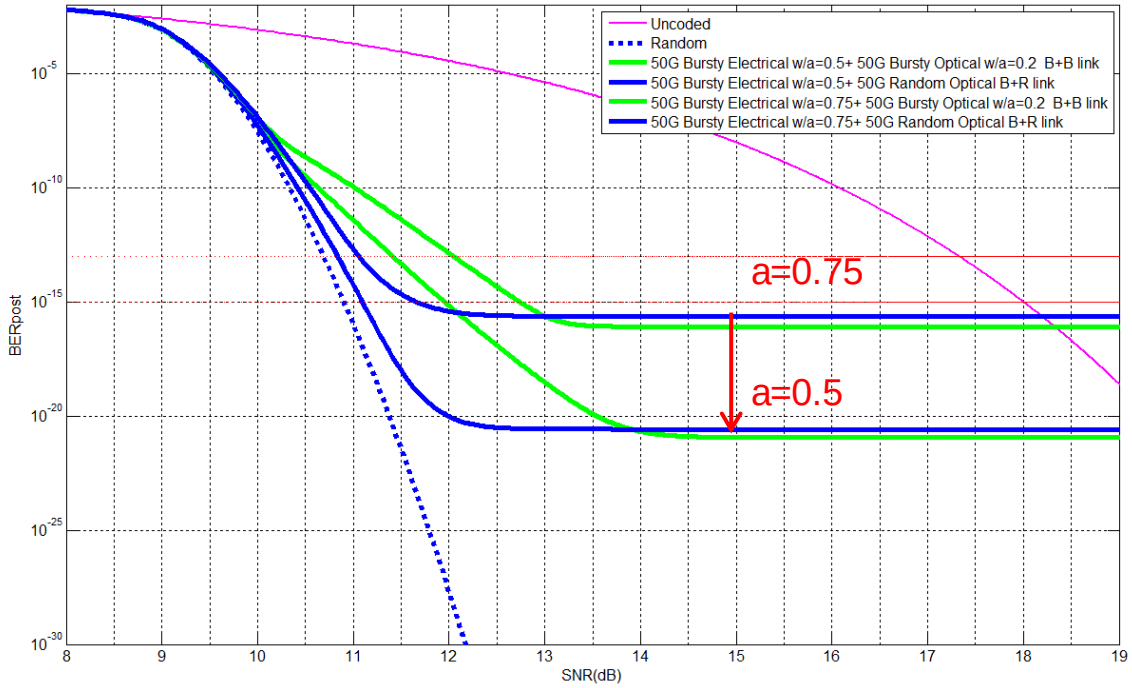
  - "PAM-4 Four Wavelength 400Gb/s solution on Duplex SMF" in conroy_3bs_01a_0914



- From silicon vendors with 2X50G PAM4 Transceiver: DFE/MLSE is included in line (Optical) side interface.

KP4 FEC Performance on PAM4 Links

- Error propagation parameter “a” of DFE will significantly shift error floor of Non-FOM Bit Mux even from 0.75 to 0.5.
- Considering burst error from optical physical link, FEC performance by Non-FOM Bit Mux will be further degraded.
- Architecture with Non-FOM Bit Mux can’t effective benefit from burst error correct capability of RS FEC.

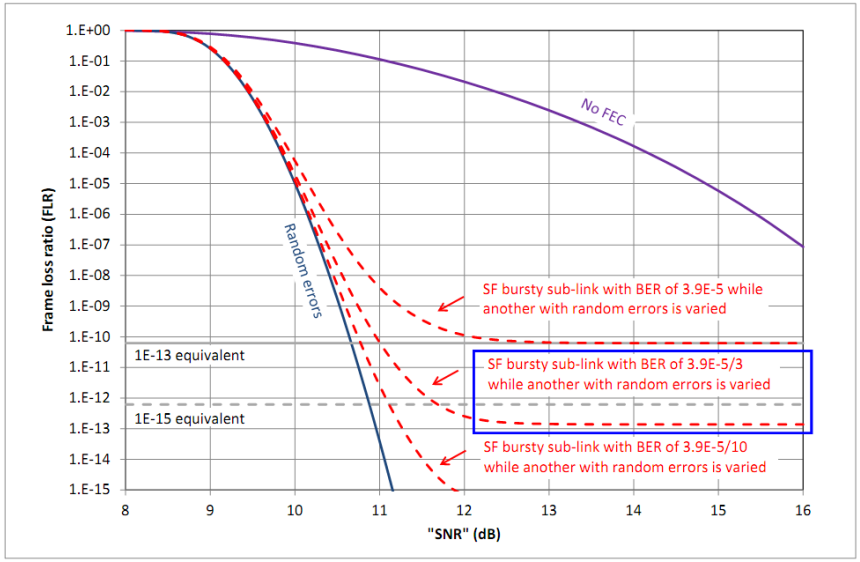


Questions Remained in FEC Performance with Non-FOM Bit Mux

- Error floor@1E-16 equivalent is showed for “Non-FOM Bit Mux” in multi part link performance for NRZ signaling.
- How about error floor in PAM4 links?
- What is the impact?

- For PAM4 signaling link, even 0.16dB borrowed from KP4 FEC(3.2dB), the 2.9E-6 is still challenge to cover up 4 electrical link as illustrative in “gustlin_3bs_02a_0515”.

RS(544,514) multi-part (1:2 SF burst + random)



anslow_3bs_02_1114

Multi-part link results

The BER of the electrical sub-links for a penalty of ~0.1 dB optical in the optical sub-link are shown in the table below.

Two alternative options for 1:2 are included: the first is for 0.1 dB optical penalty (but with little headroom for multiple electrical sub-links); the second is for 0.16 dB optical penalty (with adequate headroom for multiple electrical sub-links).

	RS(544,514) FLR = 6.2E-11			
	Electrical		Optical	
1:2 Same FEC, a = 0.75 worst skew	Burst	1.4E-6*	Random	2.4E-4
1:2 Same FEC, a = 0.75 worst skew	Burst	2.9E-6*	Random	2E-4
a = 0.75 misaligned	Burst	5.2E-6*	Random	2.4E-4
Random errors	Random	8.2E-5	Random	2.4E-4

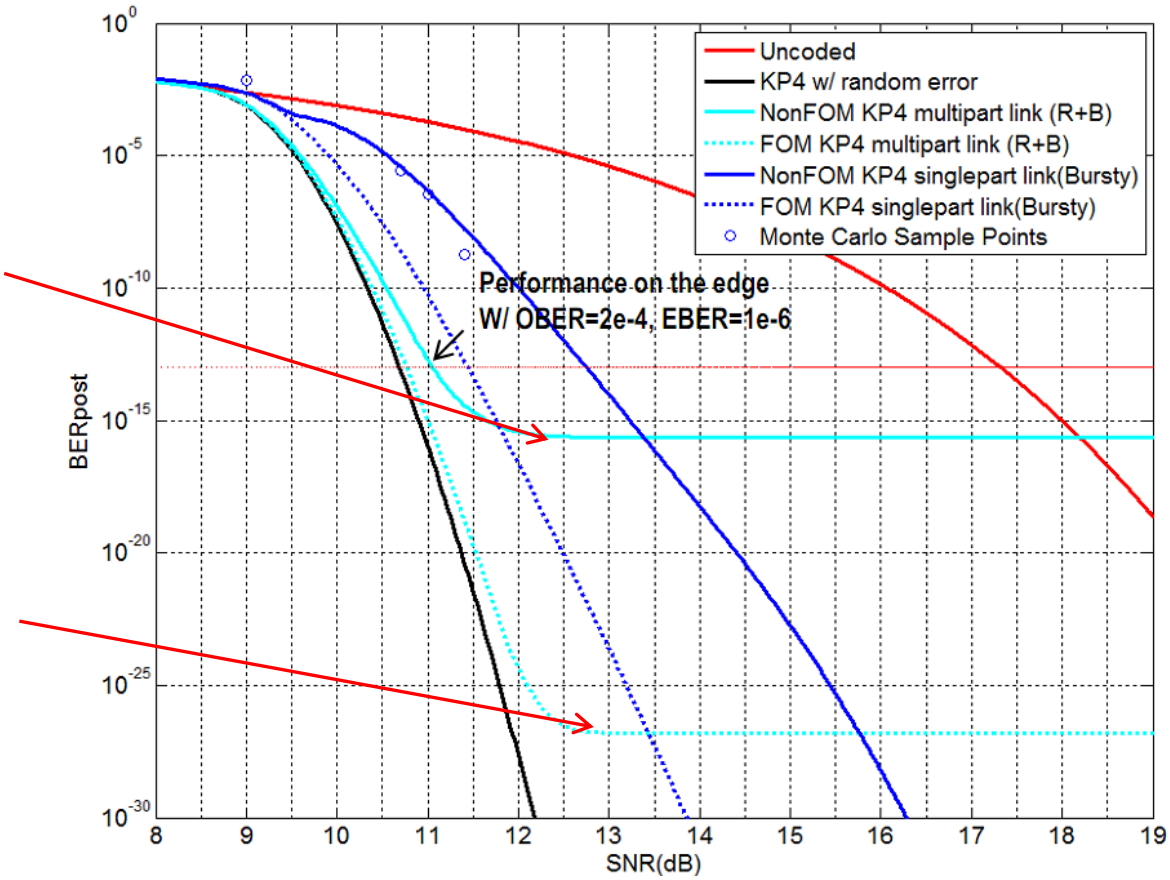
anslow_3bs_03_0515

Error Floor Issue from FEC Performance

- In "wang_t_3bs_01_0515", the following figure shows FEC performance for "Random + Bursty" link with a=0.75.

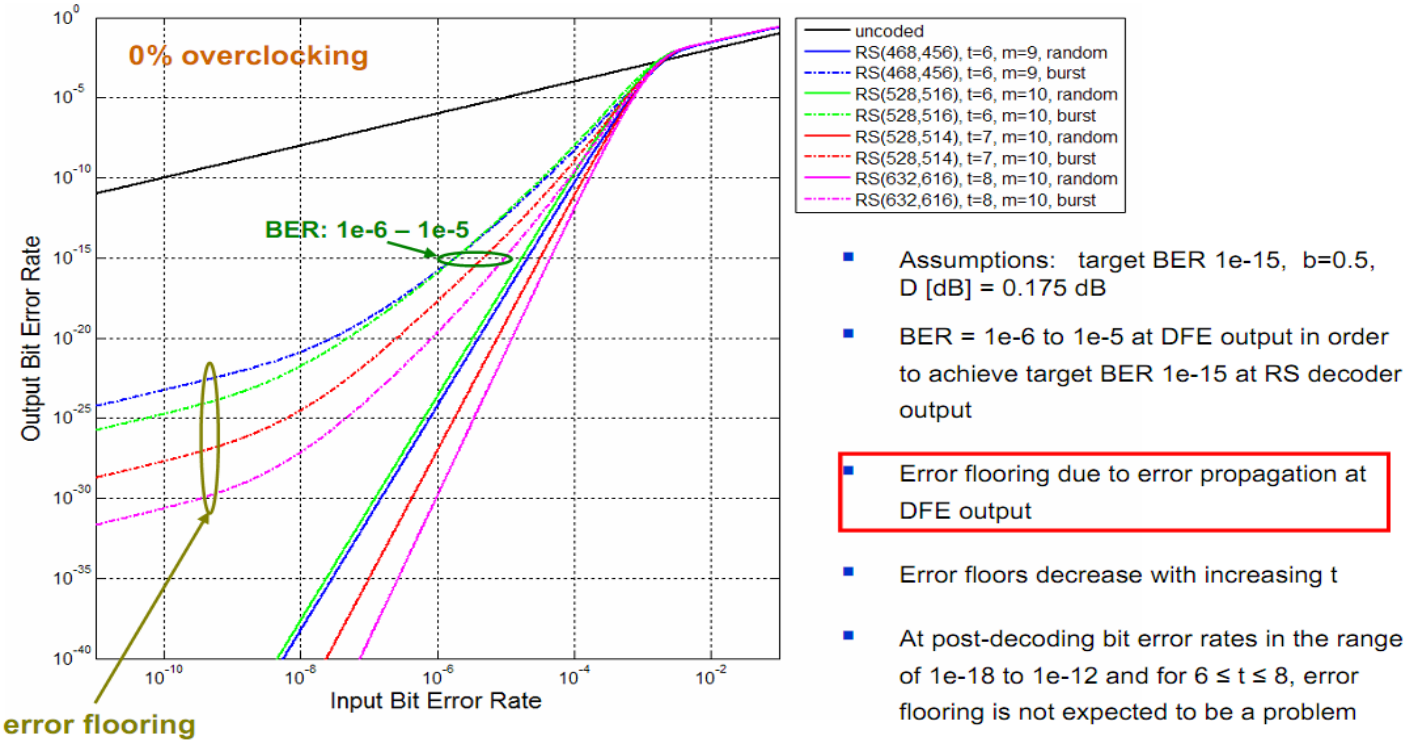
- Error floor@~1E-16 is shown in Non-FOM Bit mux scheme, starting from SNR=~12.2dB (BER=2.3E-5 on optical).

- Error floor@~1E-27 also exists for FOM bit mux, but much lower.



What Causes RS FEC Error Floor?

- In 802.3bj Project,"cideciyan_02a_1111" for symbol mux in PMA to face burst error

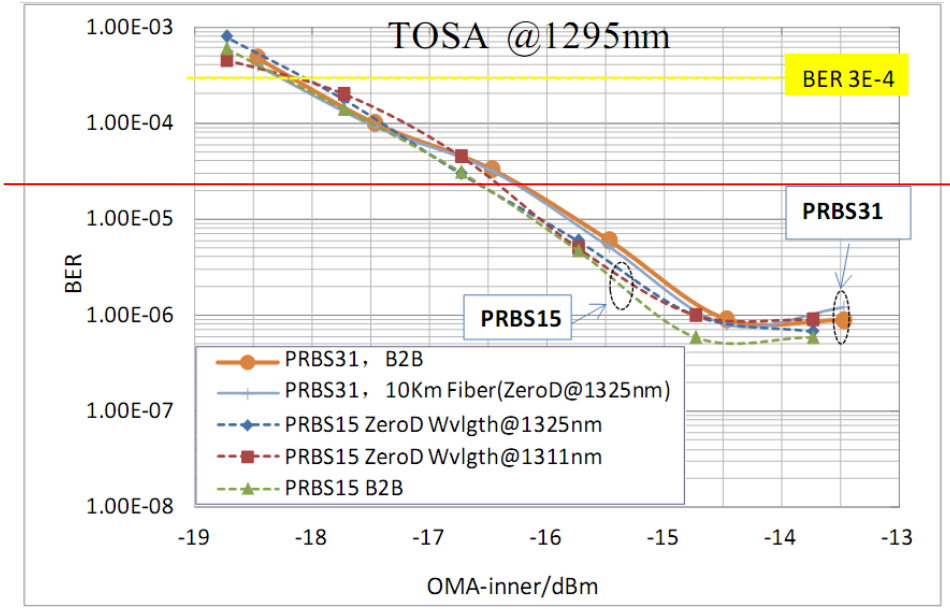


- Assumptions: target BER 1e-15, b=0.5, D [dB] = 0.175 dB
- BER = 1e-6 to 1e-5 at DFE output in order to achieve target BER 1e-15 at RS decoder output
- Error flooring due to error propagation at DFE output
- Error floors decrease with increasing t
- At post-decoding bit error rates in the range of 1e-18 to 1e-12 and for $6 \le t \le 8$, error flooring is not expected to be a problem

- Performance of Non-FOM bit mux is poor than symbol mux as in this figure.
- FEC performance in Non-FOM bit mux is much degraded and it can not be significantly improved even with only lower BER/DFE impact of electrical link.

Error Floor Issue from System Perspective

- To improve system robustness and interoperating capability, sufficient BER floor for optical physical link is required to ~1E-6 as refer to "stassar_3bs_01_0515", even when 3E-4 is enough from KP4 FEC correct capability perspective.



Penalty of DFE in electrical link by "Non-FOM Bit Mux" invalidates the margin below BER 2.3E-5 from optical link

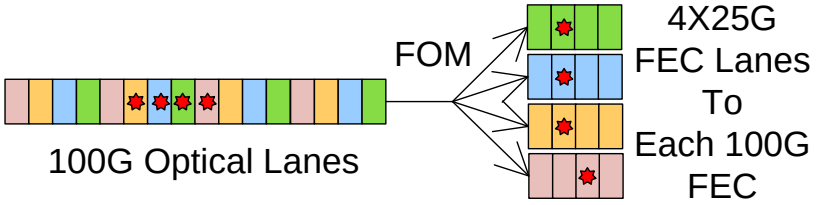
- Due to severe error floor from SNR=12.2dB aligning to BER =2.3E-5 in the above figure, the benefit of further lower BER in optical link is cancelled off by Non-FOM bit mux.
- This error floor with Post-BER at ~1E-16 can't provide sufficient margin for stable system operating, even assuming only random error from optical link.
- If some burst error in second part optical/electrical link are considered, the BER/MTTFPA will expect to fail the objective requirement of 802.3bs project.

Dilute Errors from Worst Lanes

- There is a speculation that averaging BER across multiple lanes can help add margin to the physical links with poorer performance in "anslow_3bs_03_0515". This statement is based on the following assumption:
  - To average the bad physical lanes, good lanes need to have better performance than the spec. For example, to compensate a corrupted physical link with BER > 2E-4, it requires the other lanes are operating with BER < 2E-4
    - ✓ Requiring adjacent link have better BER than specification is additional level of constrain, if one to take advantage requires clear definition in the standard
  - How many lanes with inferior BER or improved BER are allowed on each link?
    - ✓ How to account for interaction between bad/good optical and bad/good electrical lanes which may not be constructive
    - ✓ What happens when multiple lanes are working at BER limit
  - Benefits of dilution from 1x400G FEC decrease by multiple corrupted lanes or in case of fewer optical lanes.

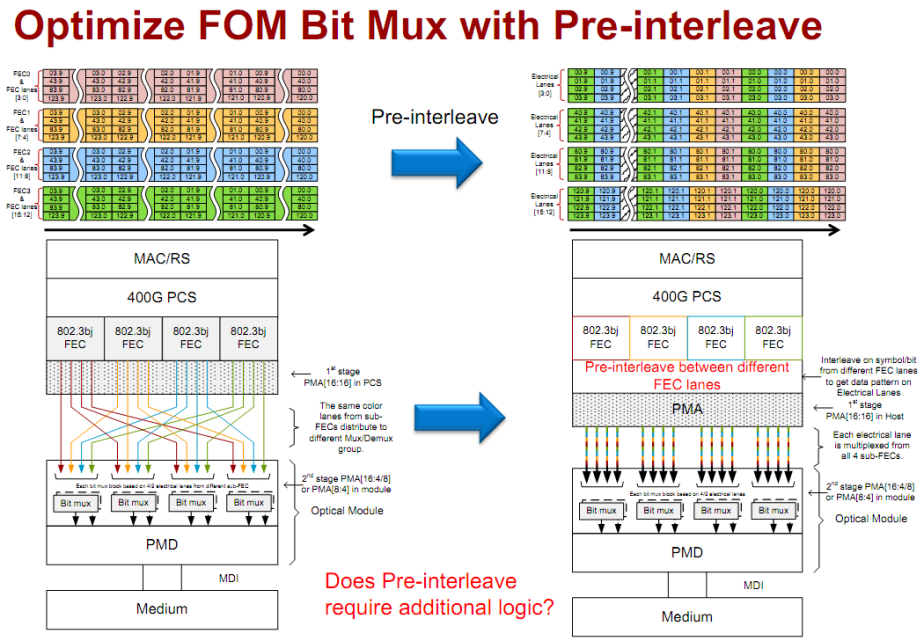
Further Analysis for “diluting the errors from the worst lane”

- How many inferior lanes operating at BER limit is legal?
  - 1,2,3,4,…… FEC Lanes? If more than 4 Lanes, 1X400G and 4X100G FEC is same even from this proposal.
- What is exactly the worst lanes in 400GbE project?
  - Is it CDAUI-16 electrical interface? The BER of CAUI-4 is 1E-15, much lower than Pre-BER level of KP4 FEC.
  - Or CDAUI-8 electrical interface or 8X optical solution, errors from physical lanes already be split to TWO FEC lanes.
  - For 4X optical solution, errors from physical lanes already be split to FOUR FEC lanes.
- Even from above error split perspective, “diluting error” is no better than “FOM” as it can’t solve burst error.



FEC Performance Enhanced by Pre-interleave

- Pre-interleave option was presented in "wang_t_3bs_01a_0115" without the complexity of wire crossing and with more consistent FEC performance
  - Better breakout support without limiting the architecture to 1 tap DFE or not supporting MLSE
- Pre-interleave also averages BER across multiple physical lanes.



Conclusion

- 1X400G FEC with bit mux even after constraining the link it may not deliver the required BER objective as result of potential burst error
  - Complex electrical-optical link BER interaction are difficult to isolate and may result in shipping products that do not robust interoperate
- 4x100G FEC with FOM bit mux
  - Offer consistent FEC performance with the need to constrain electrical or optical link
  - Can deliver 1E-15 Post-BER naturally
  - Supports DFE/MLSE likely required for future CR/KR and potentially optical PMDs
- Why risk or limit the architecture when FOM offer burst protection and ease of breakout!

Thank you

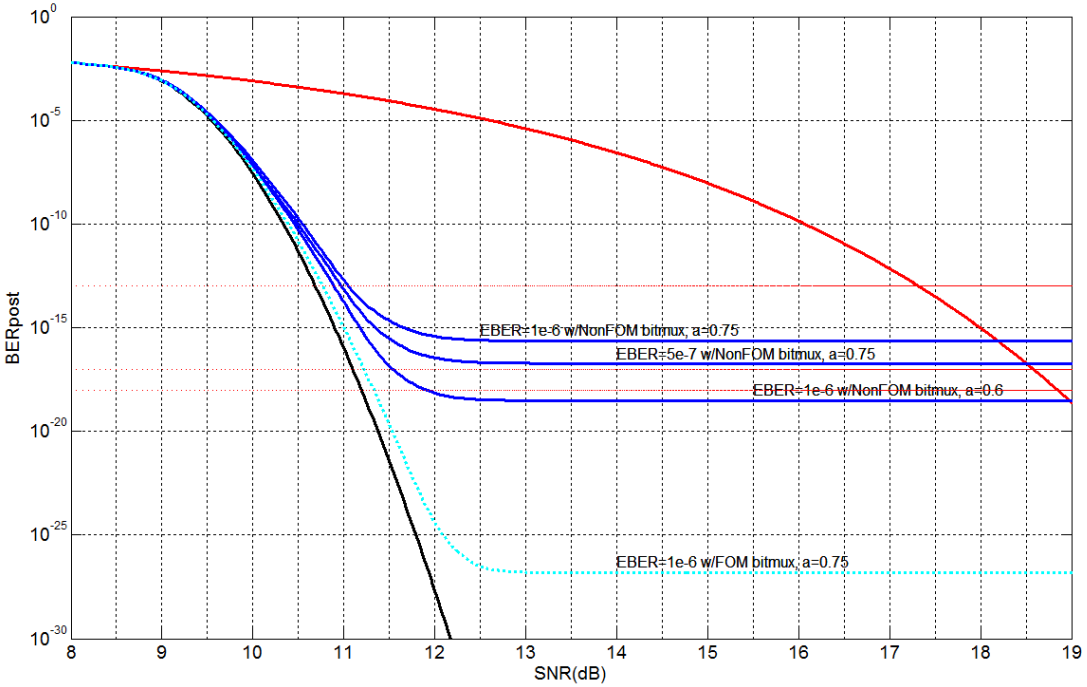
BACKUP

Error Floor Issue from FEC Performance (Cont'd)

- For further investigate the error floor and how to improve, we add the following two result for comparing.

- For relax BER of up to 4 electrical interface, we use 5E-7 as target BER, the Post-BER is ~1E-17.

- For relax error propagation by DFE with a=0.6 as an extreme case, the error floor is ~1E-18 to ~1E-19.



In Joint Slides "wang_x_3bs_01a_0115"

Coding Gain Calculation of RS(n,k,t,m) FEC

- CG/NCG is based on 802.3bs BER Objective: 1E-13
- Assuming white Gaussian noise random error only for easy analyst in this slides. Burst error just some additional penalty to CG/NCG
- Coding Gain is the reduction of raw BERin to a required BERpost value within the information signal
- Net Coding Gain is corrected to CG by the increased noise due to bandwidth expansion needed for FEC bits
- Code rate R is the ratio of bit rate without FEC to bit rate with FEC
- Transcoding to lower over-clock and improve Net Coding Gain

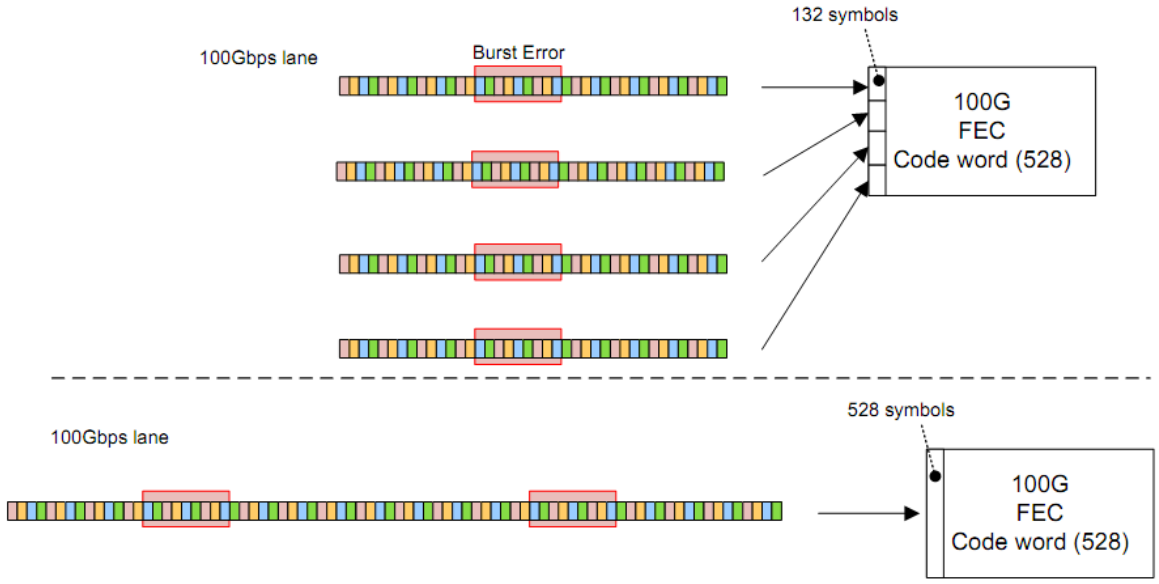
$$Coding\ Gain = 20\log_{10}[erfc^{-1}(2 * BERpost)] - 20\log_{10}[erfc^{-1}(2 * BERin)]$$

$$Net\ Coding\ Gain = 20\log_{10}[erfc^{-1}(2 * BERpost)] - 20\log_{10}[erfc^{-1}(2 * BERin)] + 10\log_{10} R$$

In "wang_t_3bs_01_0514"

Consideration on Errors From Multi-lane

- **While every lane has same error probability, errors from a single lane or from multiple lanes can be considered identically.**
  - Use $C_n^i = \binom{n}{i}$ to present the chances of having *i* errors in a codeword.



Post-BER improved by FOM Bit Mux

- As in "wang_t_3bs_01_0515", even in the following figure show FEC performance for "Random + Bursty" link with a=0.75.

- If based on BER=2E-4 in optical link to get Post BER=1E-13 objective, with the help of FOM Bit Mux, it can reach Post-BER=1E-15 to improve system robust.