Reduced-Complexity Data Alignment Scheme for 400GE

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SUPPORTERS

- To be added later

INTRODUCTION

- In [1] and [2], we already presented a new data alignment scheme which can achieve many times (>> 5x) complexity reduction in data matching operation.
- We apply the new scheme for 400GE with a small modification to the previous AM proposal [3] .
- Thus this presentation aims to present the detailed proposal for AM arrangement for 400GE

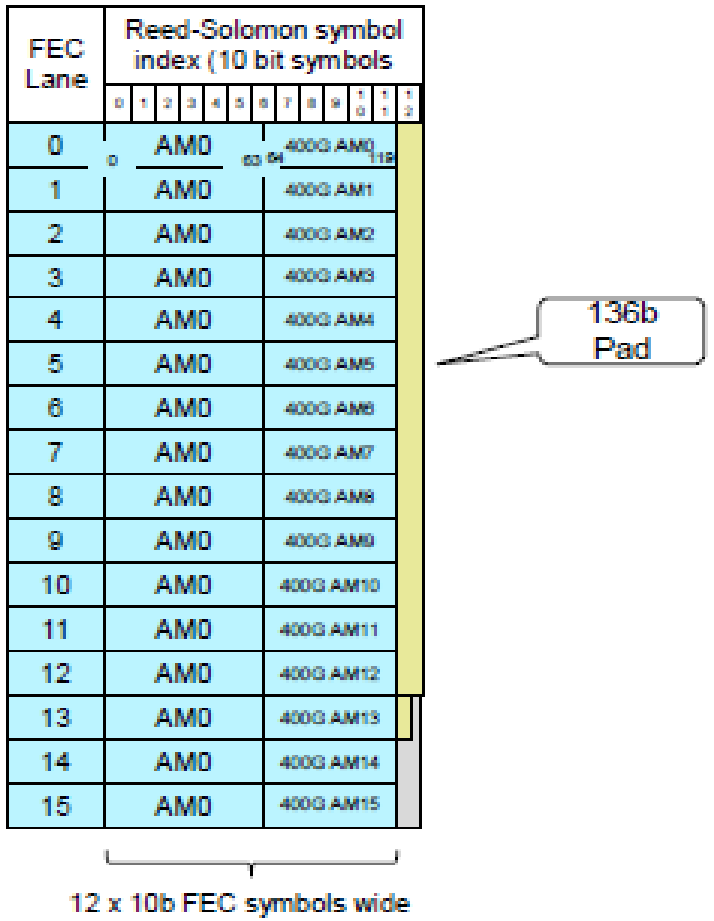
[1] http://www.ieee802.org/3/bs/public/15_05/wang_z_3bs_01_0515.pdf
[2] http://www.ieee802.org/3/bs/public/adhoc/logic/jun29_15/wangz_01_0615_logic.pdf
[3] http://www.ieee802.org/3/bs/public/15_05/gustlin_3bs_02_0515.pdf

EXISTING PROPOSAL [3]

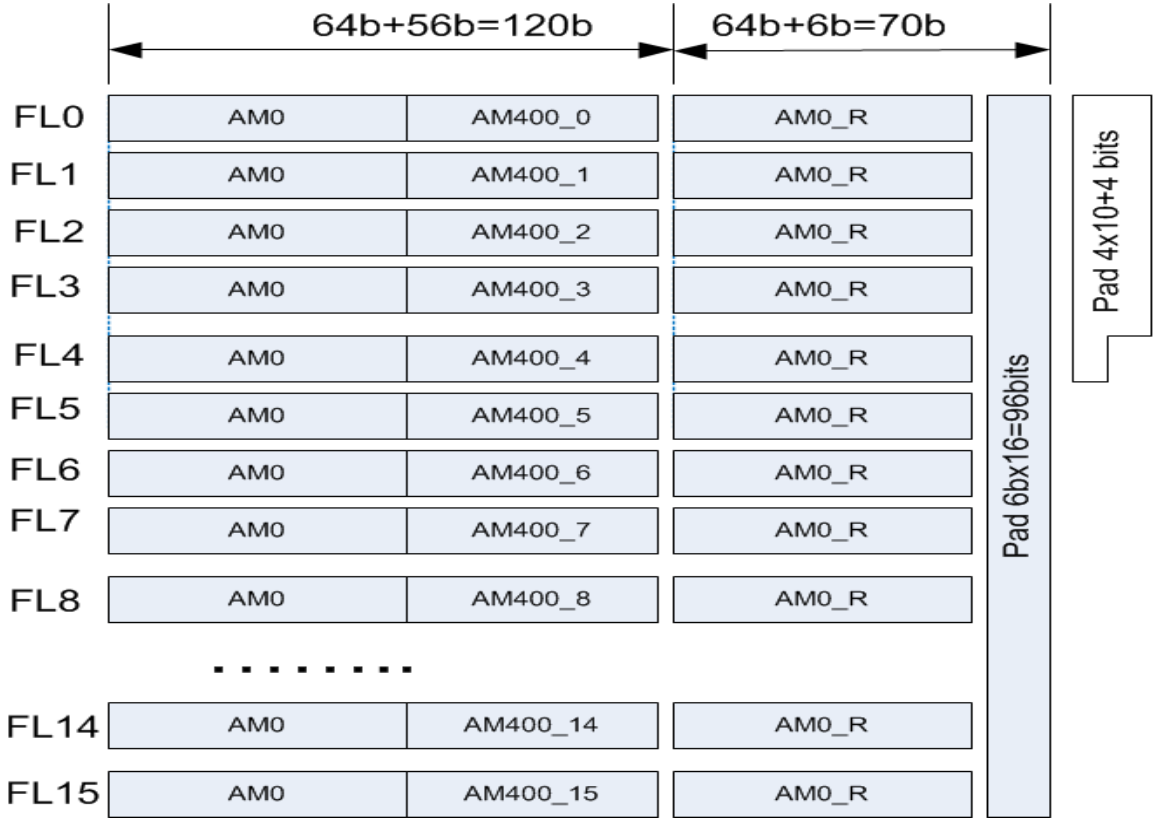
The following is “cut and paste” from [3] (page 15).

Proposed 400Gb/s AMs

- Re-use 100G AM0 from 802.3ba to allow common block lock between lanes of 100G and 400G, the rest is unique to 400GbE
- Have a 56b 400G unique AM per lane also
  - 56+64 = 120b, putting 120b on each FEC lane after RS symbol distribution requires 8x257b AM blocks
  - Content of 400G AMx is TBD

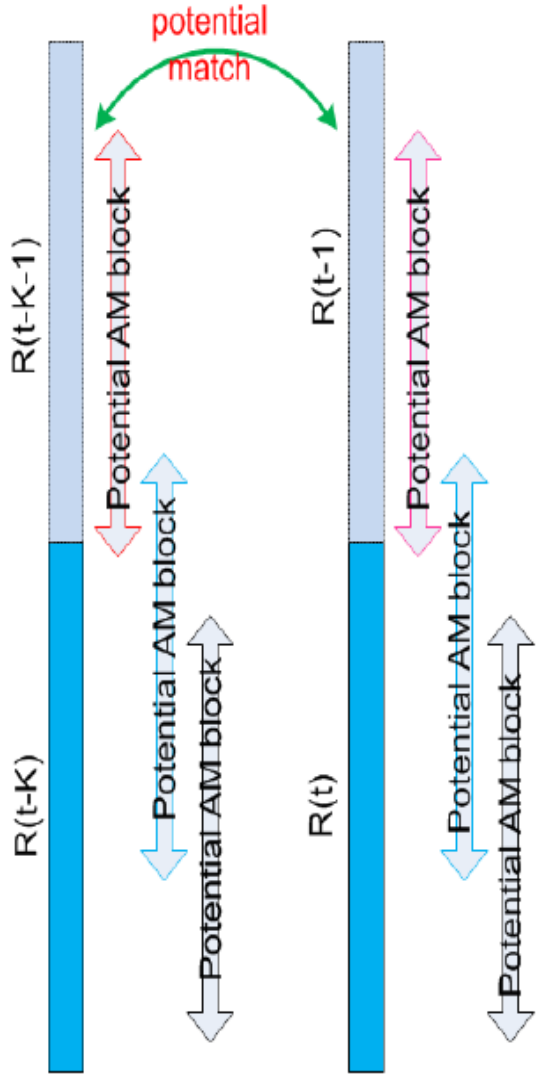


NEW AM PROPOSAL

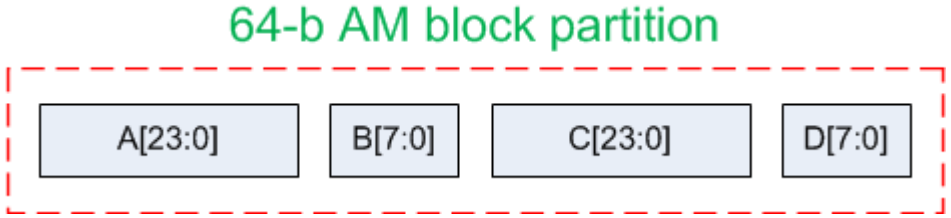


- FEC lanes 0~15 are listed in the figure as FL0 ~ FL15.
- AM400_i denotes unique i-th 400GE AM block similar as [3].
- In total, there're 190x16+44=12x257=3084 bits per AM group.
- AM0_R denotes a 64-b block. It is basically a bit-reversed version of AM0 except 8 bits.

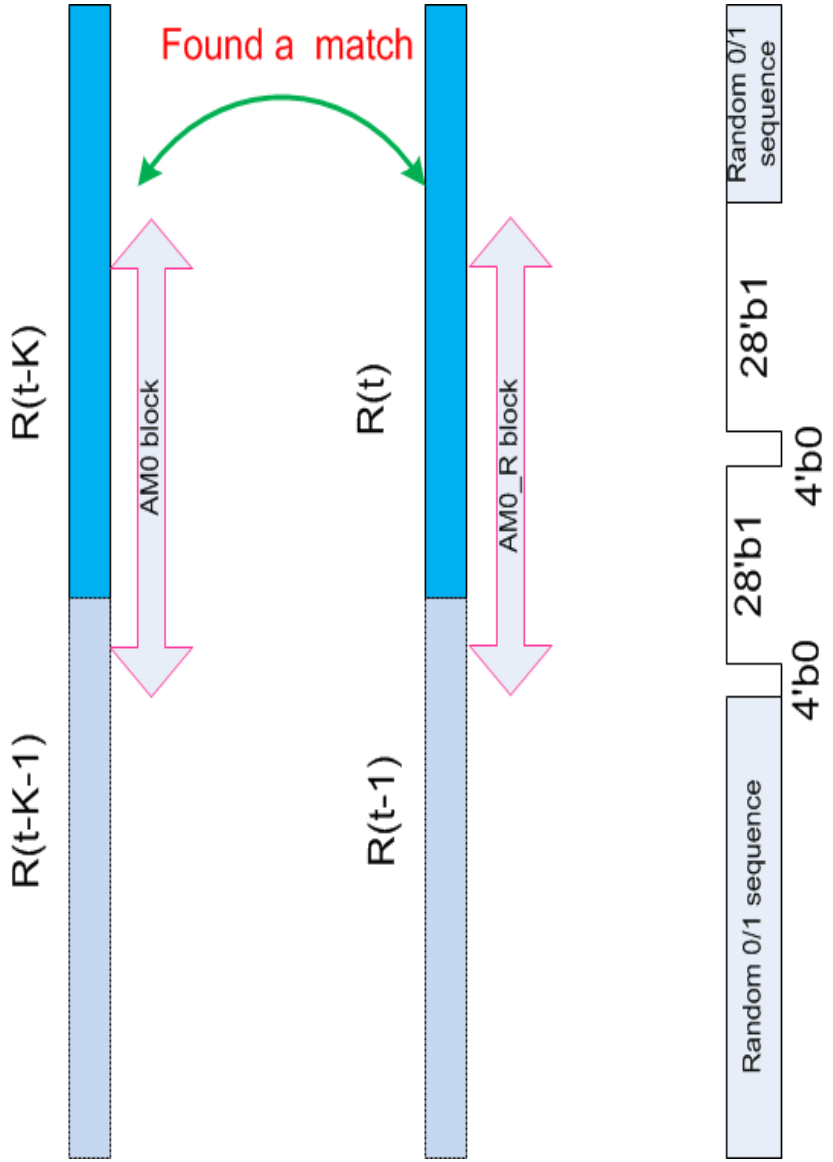
NEW AM PROPOSAL (CONT'D)



- As explained in [1] & [2], for the new scheme, we only need compare 1 case: current received vector, {R(t-1), R(t)}, vs. a past vector, {R(t-k-1), R(t-k)}.
- If there's a real match (two vectors are bit-reverse of each other), there could be n>1 extra matched bits (probability of 1/2^n) preceding the AM block.
- To ensure easy detection of AM block header, we force first 4 bits of segment A of AM0_R to be the same as those of AM0. So does the first 4 bits of segment C.



NEW DATA MATCHING EXAMPLE



- Assume there is a real match between two extended vectors: {R(t-1), R(t)} vs. {R(t-k-1), R(t-k)}.
- The result of bit-XOR of two vectors is shown on right side. If no error happens, we will see a binary sequence: start from 4 0's, then 28 1's, then another 4 0's, and followed by at least 28 1's.

ANALYSES OF NEW AM

- Assume we have 16 physical lanes. From various presentations, it is best to choose 40b/lane as buswidth for ASIC design. In this case, we actually compare R(t) vs. R(t-3).
- Assume we have 8 physical lanes. From various presentations, it is best to choose 80b/lane as buswidth for ASIC design. In this case, we also compare R(t) vs. R(t-3).
- Conventional (e.g., 80-parallel) parallel data matching method [1] can still be used in the new AM arrangement.
- Since we have 2 known AM blocks in an AM group, data alignment (or data sync.) will be faster. In general, we first check data match between {R(t-1), R(t)} vs {R(t-k-1), R(t-k)}. Then we check whether the determined 64-b AM segment (from previous matching process) match with real AM0 block.

FINAL REMARK

- We propose to modify the original AM arrangement on page 15 in [3] as what was shown on page 5 of this contribution.

- The new AM scheme have two major advantages:
  - Can enable drastic complexity reduction in hardware implementation,
  - Can speed up data synchronization process.