# Chief Editor’s report

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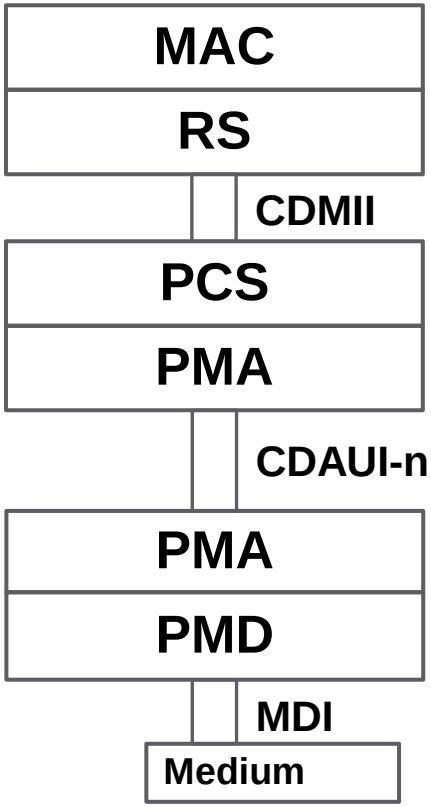
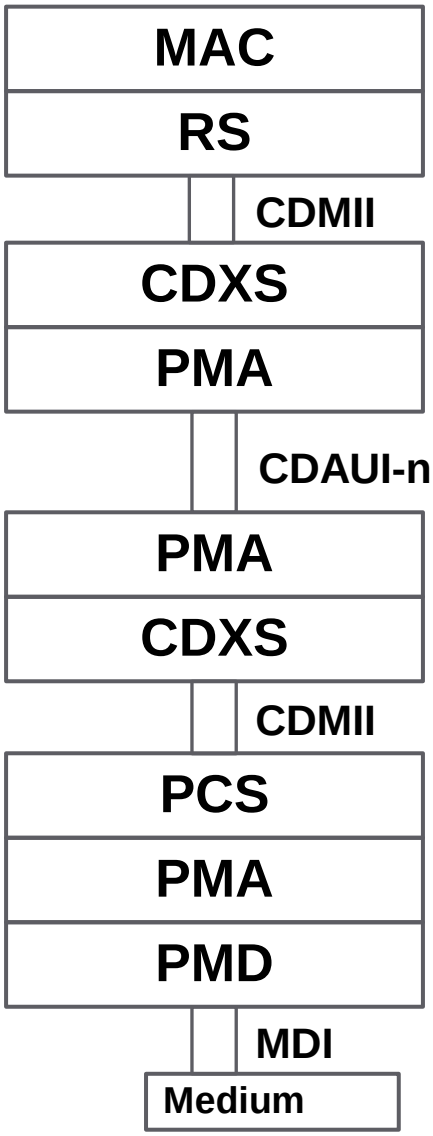
# Introduction

The following slides contain:

- the structure of the P802.3bs 400 Gb/s Ethernet draft amendment
- list of editors
- a list of open questions for adopted baselines

# Adopted stack




When PCS functions and CDXS functions do not match

# New clauses

| Clause | Content | Baseline |
|---|---|---|
| 116 | Introduction to 400 Gb/s networks | |
| 117 | RS and MII for 400 Gb/s operation | |
| 118 | CDMII extender (includes CDXS) | Baseline adopted |
| 119 | PCS including FEC | Baseline adopted<br>PCS lane striping TBD |
| 120 | PMA | Baseline adopted |
| 121 | 400GBASE-SR16 | Baseline adopted |
| 122 | 400GBASE-DR4 | Baseline adopted |
| 123 | 400GBASE-FR8 and 400GBASE-LR8 | Baselines adopted |
| 120A | Partitioning examples (informative) | |
| 120B | CDAUI-16 chip-to-chip (normative) | Baseline adopted |
| 120C | CDAUI-16 chip-to-module (normative) | Baseline adopted |
| 120D | CDAUI-8 chip-to-chip (normative) | Baseline adopted |
| 120E | CDAUI-8 chip-to-module (normative) | Baseline adopted |

# Amended clauses

| Clause | Change | |
|---|---|---|
| 1 | Add new references, definitions, abbreviations | |
| 4 | Add 400G parameters to Table 4-2 | |
| 30 | Add new management objects / attributes | |
| 45 | Add new registers / bits | |
| 78 | Add new EEE PHYs | Baseline adopted |
| Annex A | Add any new bibliography entries | |
| Annex 4A | Add / modify note to Table 4A-2 | |
| Annex 31B | Add 400G PAUSE information | |
| Annex 93A | Modify Table 93A-2 | |

# Editorial team

Pete Anslow, Ciena

- Chief Editor and Editor for Clauses FM, 00, 1, 4, 30, 45, 78, 116, A, 4A, 31B, 93A, 120B, 120C

Mark Gustlin, Xilinx

- Editor for Clauses 117, 118, 119

Steve Trowbridge, Alcatel-Lucent

- Editor for Clause 120, 120A

Jonathan King, Finisar

- Editor for Clause 121

Peter Stassar, Huawei

- Editor for Clauses 122, 123

Andre Szczepanek, Inphi

- Editor for Annexes 120D, 120E

# Open questions for PCS and PMA

- How are the PCS lanes formed from the FEC code words?
  - Does this affect the assumption of blind bit-multiplexing in the PMA?
- Use FEC metrics for defining hi_ber threshold?
- PCS sublayer delay constraints and skew values are “magenta”
- 400G AM fields are TBD
- What criteria should be used for AM lock?
- PMA generated test patterns
  - Best guess will be included in the draft
- MMD Device Numbering
  - Can we reduce to three maximum PMA instances per end since there is no stand alone FEC separate from the PCS?
  - How does CDXS affect MMD device numbering?

# Open questions for 400GBASE-SR16

- BER requirement given RS(544,514,10) FEC and sharing of the BER budget with electrical interfaces.
- Adoption of RS(544,514,10) FEC increases the signaling rate from 25.78125 GBd for 100GBASE-SR4 to 26.5625 GBd.  What changes are needed to the specification to account for this?

# Open questions for 400GBASE-DR4/FR8/LR8

- Definition of OMA for a PAM4 modulation format
  - Are two definitions needed, one for inner and the other for outer?
  - Alternatively, is it better to define only outer OMA and control inner eye uniformity via a penalty?
- TDP (Transmitter and Dispersion Penalty) is used to control transmitter eye quality and spectral characteristics for single-mode PMDs such as 100GBASE-LR4.
  - How will this be done for a PAM4 transmitter in 400GBASE-DR4/FR8/LR8?
  - What should the specification for the reference receiver be?
- Stressed receiver sensitivity
  - How should the stressed signal be generated?
  - How should the amount of stress in each sub-eye be controlled?
- For 400GBASE-DR4
  - What are the MDI requirements?

# Open questions for CDAUI-16

Chip-to-chip and chip-to-module

- BER requirement is TBD
- Adoption of RS(544,514,10) FEC increases the signaling rate from 25.78125 GBd for CAUI-4 to 26.5625 GBd. What changes are needed to the specification to account for this?

Chip-to-module

- CDAUI-16 will need a 16 way connector instead of a 4 way connector. Are there any changes required to the specification to account for this?
- Annex 83E for CAUI-4 chip-to-module requires that the host provides a “recommended CTLE peaking value”. There was some discussion before the baseline was adopted as to whether this would also be required for CDAUI-16.

# Open questions for CDAUI-8

- COM parameter TBDs
- Is there a need to restrict the probability of a burst continuing to be below 0.75?

Thanks!