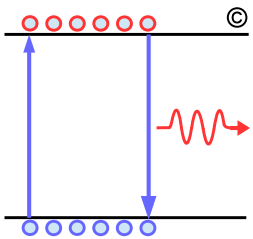


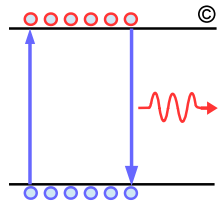
Options for CRU BW for 400 GbE PAM4 PMDs

Ali Ghiasi
Ghiasi Quantum LLC

802.3bs Electrical Meeting

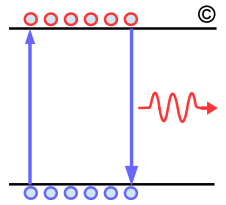
Sept 14, 2015

List of Supporters



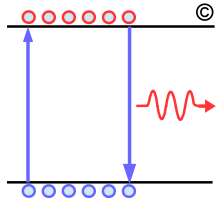
- Gary Nicholl – Cisco Systems
- Marco Mazzini – Cisco Systems
- Andre Szczepanek – Inphi Inc
- Magesh Valliappan – Broadcom Inc
- Mike Dudek – Qlogic
- Edward Frlan – Semtech
- Bharat Tailor - Semtech

Overview

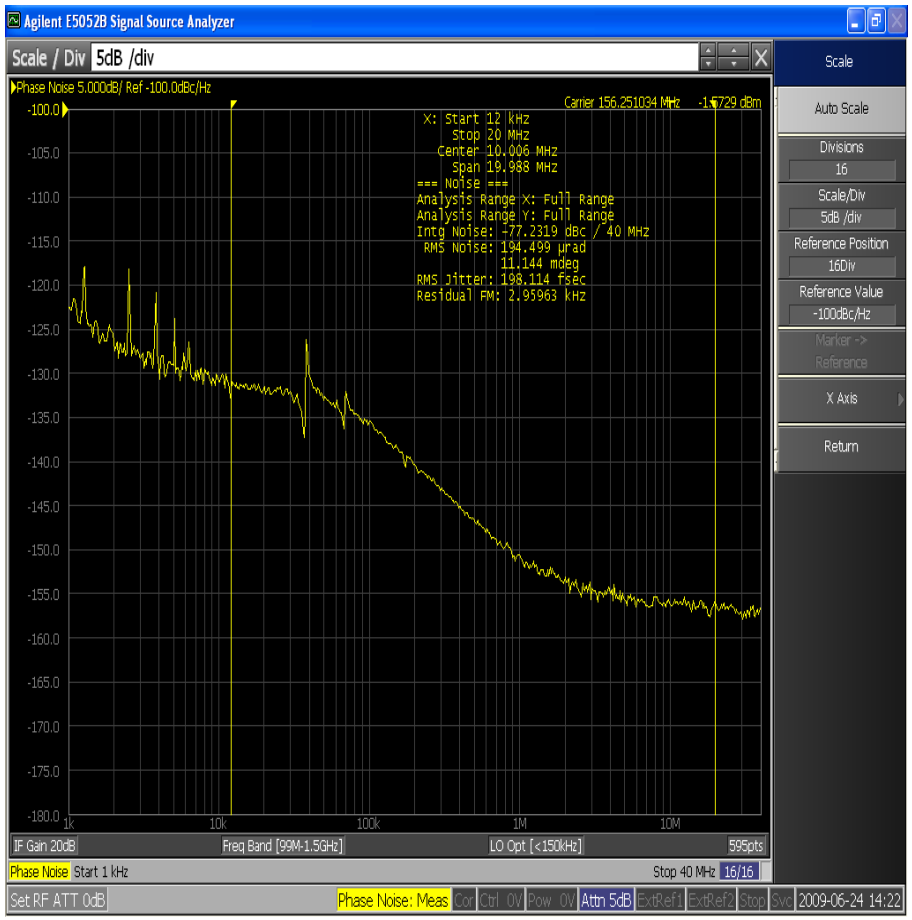


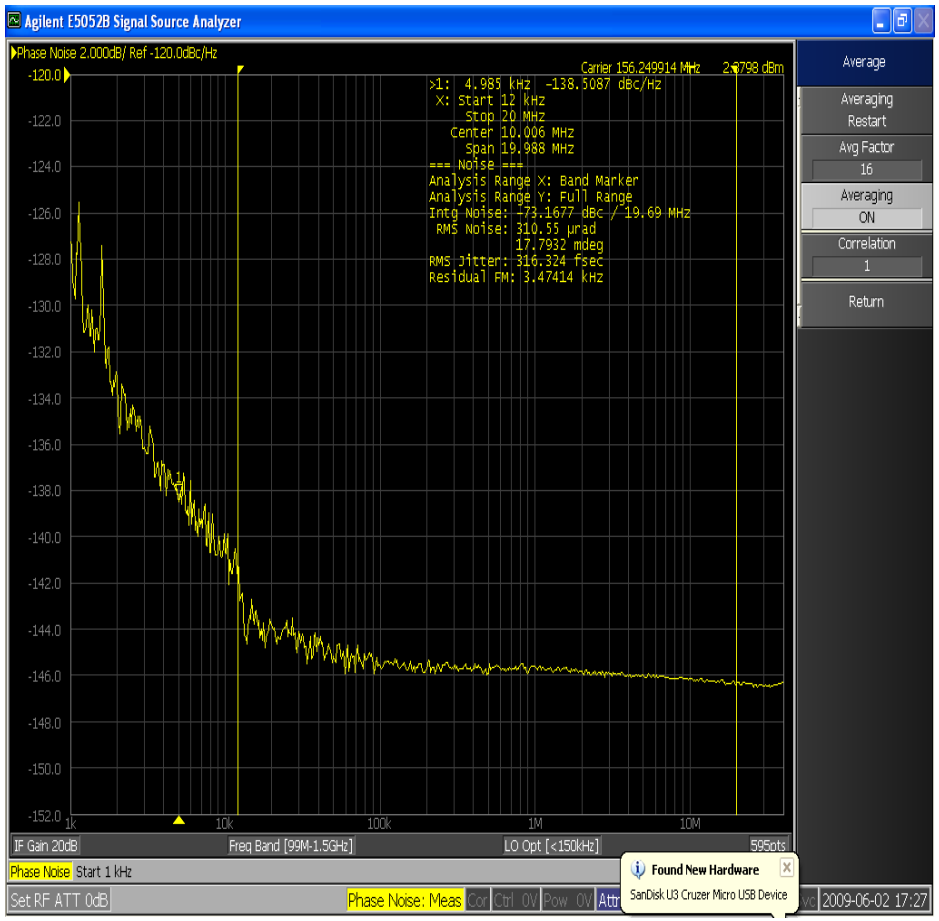
- **Previously considerations for CRU and CDR BW have been presented in details**
  - http://www.ieee802.org/3/bm/public/mar14/ghiasi_01_0314_optx.pdf
  - http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf
  - http://www.ieee802.org/3/ba/public/jan10/ghiasi_01_0110.pdf
- **802.3bs has no specific objective for a ports to be backward compatible with legacy 10 GbE, 40 GbE, or 100 GbE**
  - Since 802.3ae in Ethernet we have been using CRU BW of Fbaud/2578
  - CRU BW for standards at 10.3125 GBd/lane is 4 MHz
  - CRU BW for standards at 25.78 GBd/lane is 10 MHz
  - The market however requires at least the host provide a level of backward compatibility
  - CDAUI-16 based on 4 instance of CAUI-4 carries forward 10 MHz CRU
- **Next will explore OSC/VCO phase noise and options for 802.3bs CRU BW.**

Typical Low Cost Oscillator Phase Noise Plot (from ghiasi_01_0110.pdf)

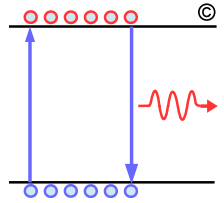


- As the phase plot show there was no benift having CRU BW>1 MHz

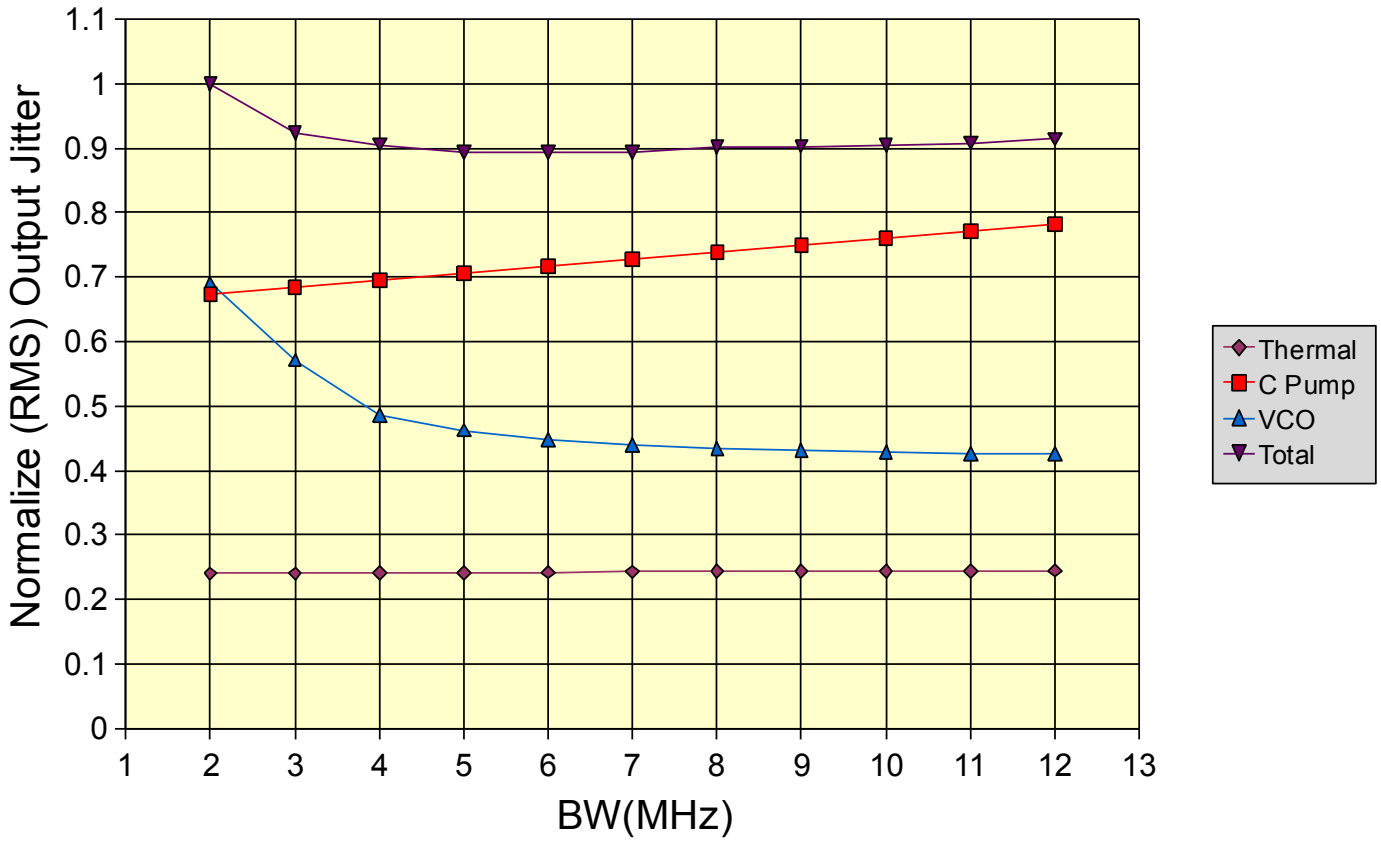




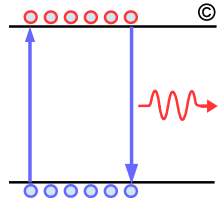
SerDes Transmitter Relative Jitter (from ghiasi_01_0110.pdf)



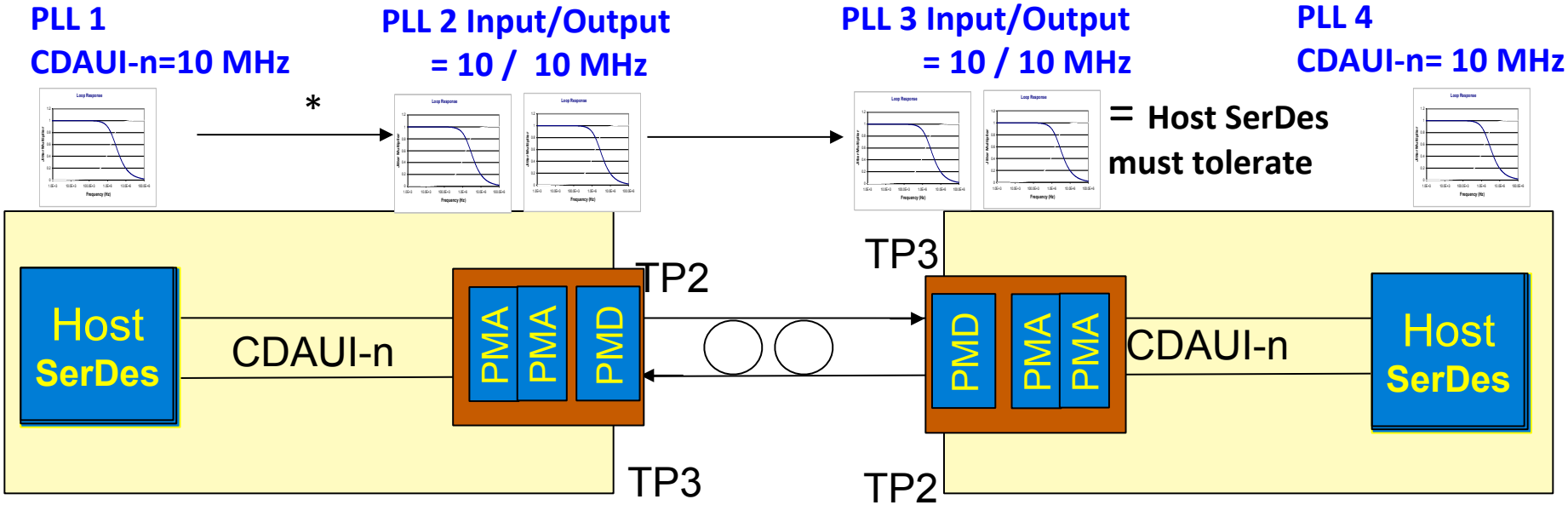
- **Thermal, charge pump, VCO, and total relative output jitter as function of BW**
  - CRU> 4MHz provide no measurable able benefit but for BW> 10 MHz charge pump noise start dominating



Option 1: Assume 10 MHz CRU BW

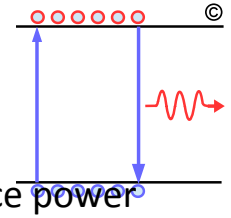


- **Propose to use 10 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8**
- **It simplifies the overall architecture at expense of requiring faster tracking BW resulting in higher power on more complex PAM4 receivers**
  - This approach is backward compatible with previous IEEE standards and compatible with CDAUI-16 which is based on CAUI-4
  - Allow implementation to follow current 100G retime modules based on CAUI-4 based on simple CDR without FIFO (insertion/deletion or phase) when # of in/out lanes equal.

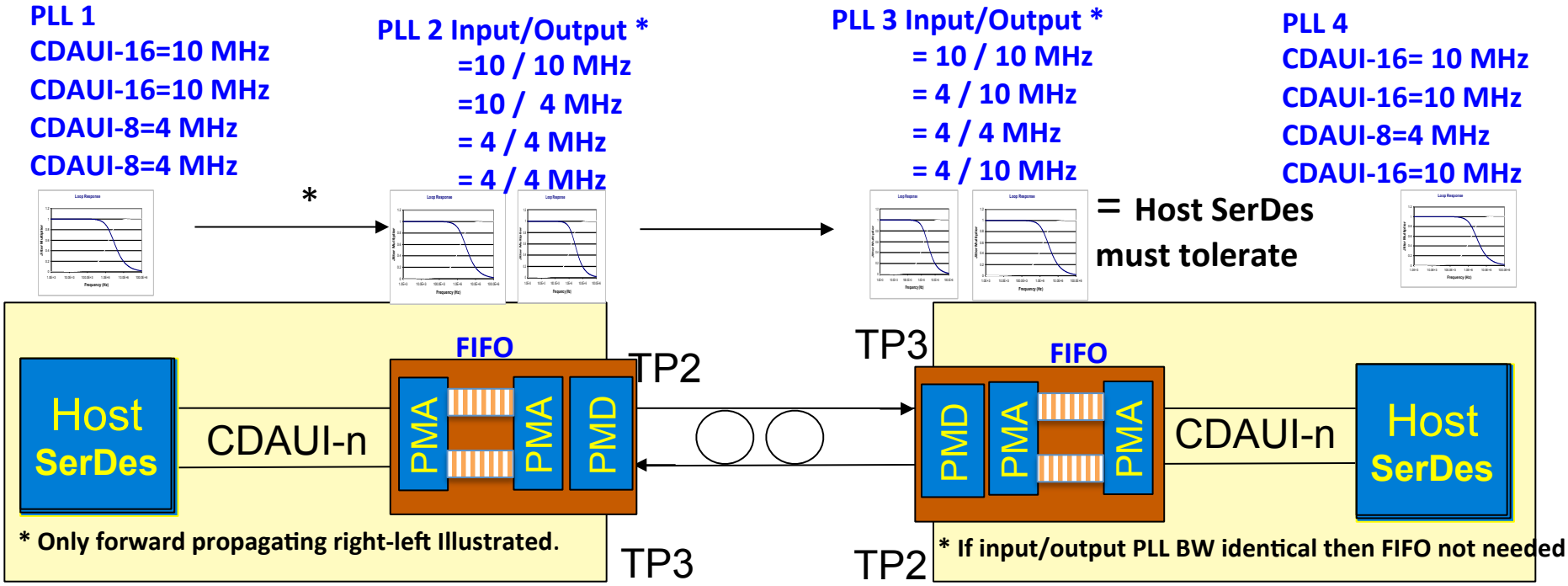


* Only reverse propagating right-left not illustrated would be similar.

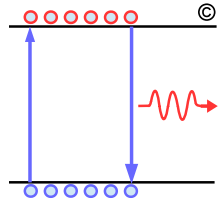
Option 2: Assume 4 MHz CRU BW



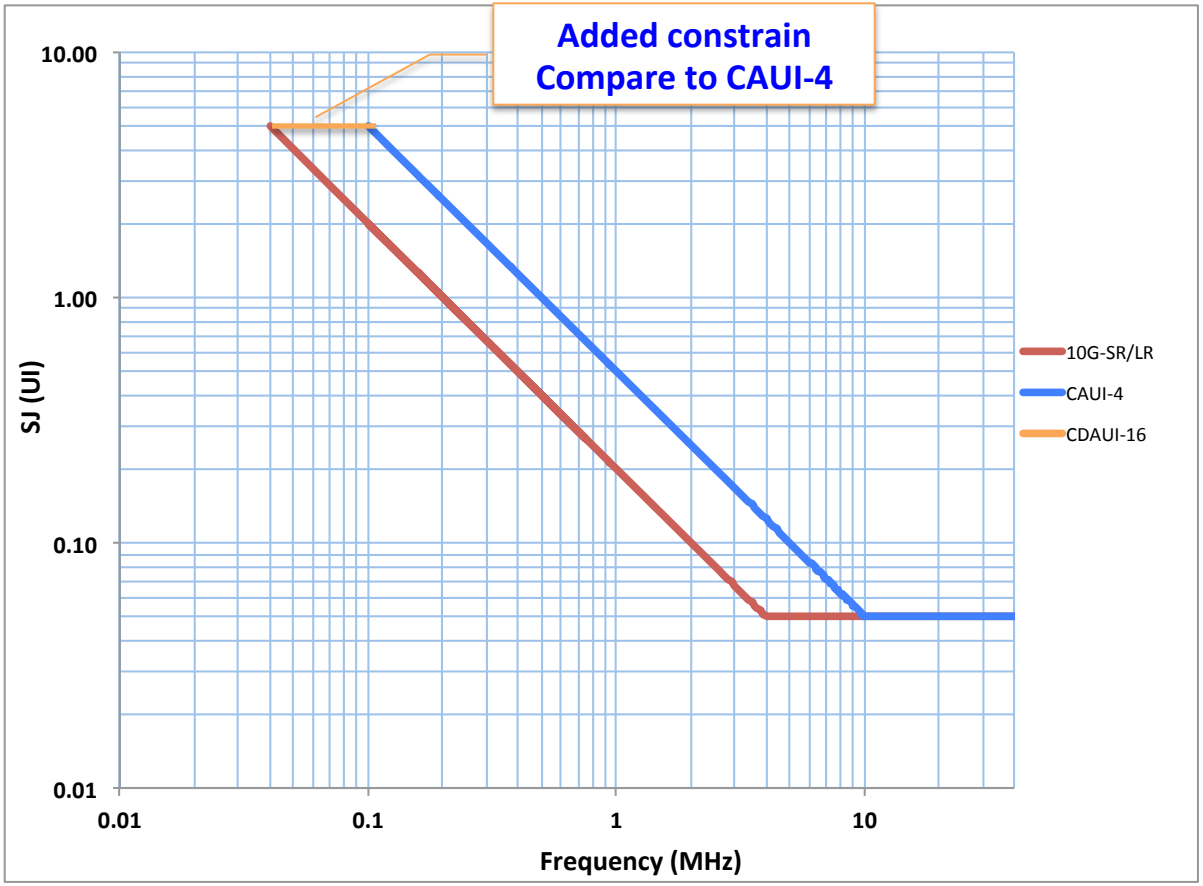
- **Propose to use 4 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8**
  - Backward compatible with 10.3125 GBd/lane PMD's
  - 4 MHz tracking BW could benefit more complex PAM4 Cu/MMF receivers and reduce power
- **This approach is not fully backward compatible with IEEE standards operating 25.78 GBd/lane or CDAUI-16 which is based on CAUI-4 but manageable**
  - Require a PMA-PMA chip in the module with FIFO or a dual loop PLL
    - Anytime number in/output lanes not equal or at destination FIFO required for differential skew
  - Module PMA does not need FIFO in case of CDAUI-8 host in conjunction with 8 lanes PMDs
  - CDAUI-8 host operating with legacy host based on 25.78 GBd/lane require a PMA-PMA chip with FIFO and/or dual loop PLL
    - To make this option work without insertion/deletion FIFO wander from 100 KHz to 40 KHz must be addressed.



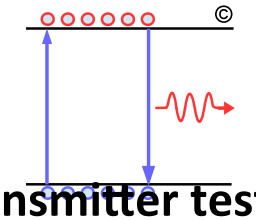
How to Deal with Wander from 40 kHz-100 KHz



- **CAUI-4 10 MHz CRU does not define wander from 40 kHz-100 kHz where 4 MHz CRU are defined down to 40 kHz**
  - Need to add 5 UI wander generation from 40 KHz-100 KHz on CDAUI-16



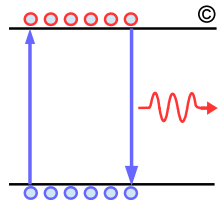
Summary



- **Reliable link operation requires that the receiver test complements transmitter test**
  - Golden CRU having high pass response mask the transmitter low frequency jitter components propagating down the link that the receiver must tolerate
- **HOM receivers are more complex with timing recovery potentially having higher latency could make it difficult to support Fbaud/2578 CRU**
  - CDAUI-16 based on CAUI-4 forces 10 MHz CRU into the 802.3bs
    - Adding 5 UI wander generation from 40-100 KHz on CDAUI-16 ports will simplify implementation of CDAUI-8-CDAUI-16 without the need for insertion-deletion FIFO
  - If input/output lanes are not equal or at termination SerDes FIFO is required to absorb dynamic skew and could also be designed to absorb 10 MHz CRU jitter
- **Two viable options explored are:**
  - Option I: 10 MHz CRU BW for all 50/100 Gb/s PAM4 PMDs allow full backward compatibility with CDAUI-16 as well as legacy PMD support but at expense of power and possibly limiting the implementation
  - Option II: 4 MHz CRU BW for all 50/100 Gb/s PAM4 PMDs with low frequency wander constrain the CDAUI-16 ports to eliminates the need for insertion/deletion FIFO and provide backward compatibility
    - PAM4 PMAs interoperating with legacy NRZ PMDs with open eye likely will have full tracking BW
- **10 MHz CRU BW could be challenging considering future more complex HOM PMDs but we know how to deal and manage 4 MHz CRU**
- **What ever we choose for CRU BW the receiver must operate with stress with jitter components masked by the transmit CRU high pass response.**

Editor Notes

(Suggestions provided by Author not yet reviewed by the supporters)



Add text to 122.8.8, 123.8.8 (Transmitter optical waveform)
120D.3.1 (CDAUI-8 transmitter characteristics)
120E.3.1 **CDAUI-8 host output characteristics**
"All transmitter measurements are made with a clock recovery unit (CRU) with a corner frequency of 4 MHz and a slope of 20 dB/decade."

120B.3.1 CDAUI-16 chip-to-chip transmitter characteristics
A CDAUI-16 chip-to-chip transmitter shall meet all specifications in 83D.3.1 with the exceptions that the signaling rate per lane is 26.5625 Gbd ± 100 ppm and "maximum wonder jitter generation from 40kHz-100 KHz limited to 5 UI"……

120C.3.1 CDAUI-16 host output characteristics
A CDAUI-16 host output shall meet all specifications in 83E.3.1 with the exception that the signaling rate per lane is 26.5625 Gbd ± 100 ppm and "maximum wonder jitter generation from 40kHz-100 KHz limited to 5 UI" .

Editor Notes

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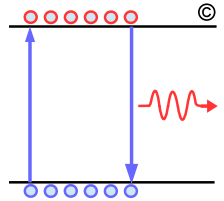

Add text to 122.8.10, 123.8.10, Stress Receiver Sensitivity or subsection

"**Sinusoidal jitter for receiver conformance test**

The sinusoidal jitter is used to test receiver jitter tolerance. The amplitude of the applied sinusoidal jitter is dependent on frequency as specified in Table below"

120D.3.3.2 Receiver Jitter tolerance

The receiver shall operate over the full range of sinusoidal jitter tolerance in table below with method Described…

The parameter in table 120D-6 is are two suggested test case at frequency of 40 kHz and 4 MHz (or Value of can be listed in Fabud).

120E.3.3.2 Host Stress Input and 120E.3.4.1 Module stress input

change 10 MHz with 4 MHz

Table 120E-4 change reference to Table in CL 88-13 with 10 MHz CRU to table below

Frequency range	Sinusoidal jitter peak-to-peak (UI)
f < 40 kHz	Not specified
40 kHz < f ≤ 4 MHz	$2\times 10^5/f$
4 MHz < f ≤ 10 *Lb*[1]	0.05

1. loop bandwidth; upper frequency bound for added sinusoidal jitter should be at least 10 times the loop bandwidth of the receiver being tested.