FEC Latency for Interleaving Schemes

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Outline

- FEC Architecture and Latency Review
- Latency of Pre-interleaving Schemes
- Latency of FOM

Review - FEC Latency and Complexity

- **Decoder Latency ([1] sun_3bs_01_0715)**
  - no interleaving, no breakout

FEC Architecture	1x400G KP4
1x400G FEC Latency(ns)	72
2x200G FEC Latency (ns)	84
4x100G FEC Latency (ns)	110

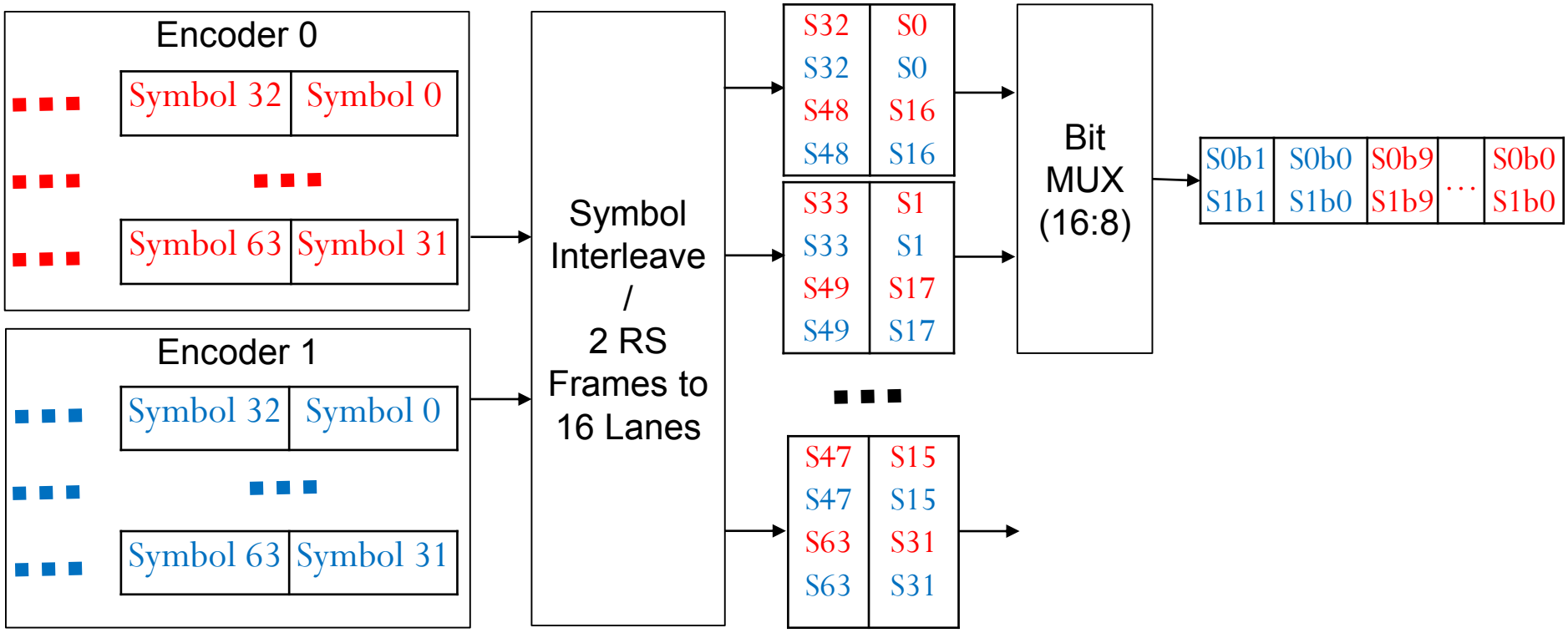
- **Encoder Latency**: ~3ns for all cases.

- **Corresponding Complexity**:
  - CS latency is targeted to 8 cycles for all FECs.
  - Relative complexity is listed for all major blocks.
  - No big difference in hardware cost.

FEC Architecture	Encoder	Syndrome	KES	CS	Forney
1x400G FEC	4.5x	4.4x	4x	1	4.4x
2x200G FEC	4x	4x	4x	2	4x
4x100G FEC	4x	4x	4x	4	4x

2-way symbol interleaving

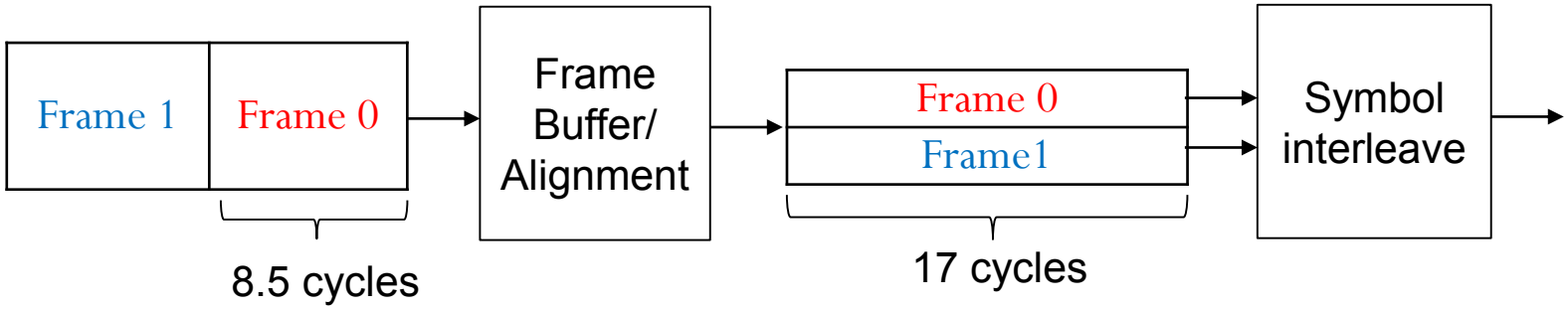
- **Scheme 8 in [2]** anslow_01_0815_logic
- **For 2x200G FEC with 320 bit buswidth**:



- **Latency : 87ns.**
  - 3ns for encoder + 84ns for decoder.
  - No extra latency for interleaving.
  - For odd FEC lanes, the order of blue and red symbols can be swapped.

2-way symbol interleaving

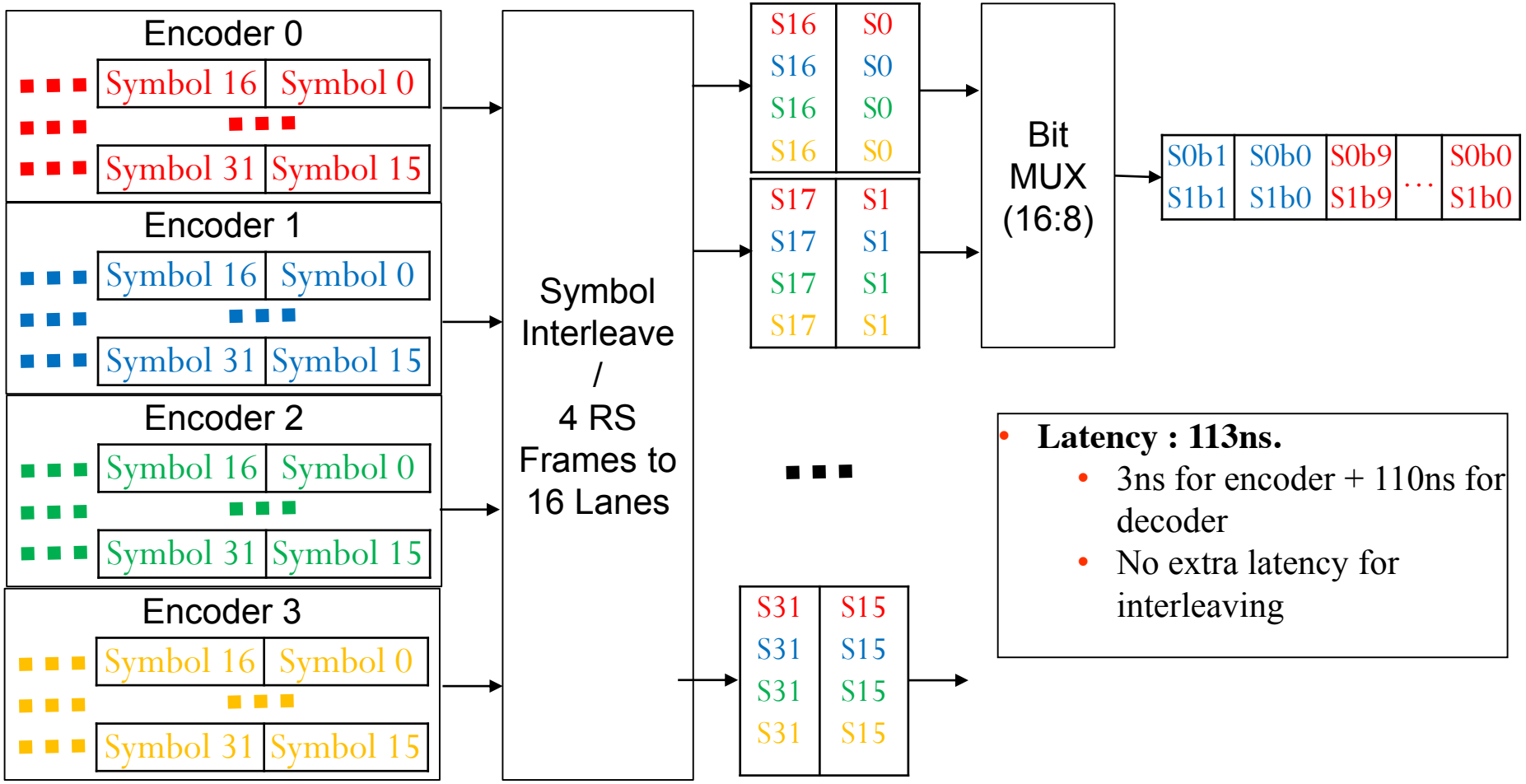
- **For 1x400G FEC with 640 bit buswidth**:
  - Symbol interleaved from 2 serial frames



- **Latency:**
  - 8 extra cycles on both encoder and decoder sides to align frames.
  - **75+12+12=99 ns.**
- **Complexity**: ~3x5K bit extra memories
  - 1.5x5K memories on both encoder and decoder sides to buffer frames

4-way symbol interleaving

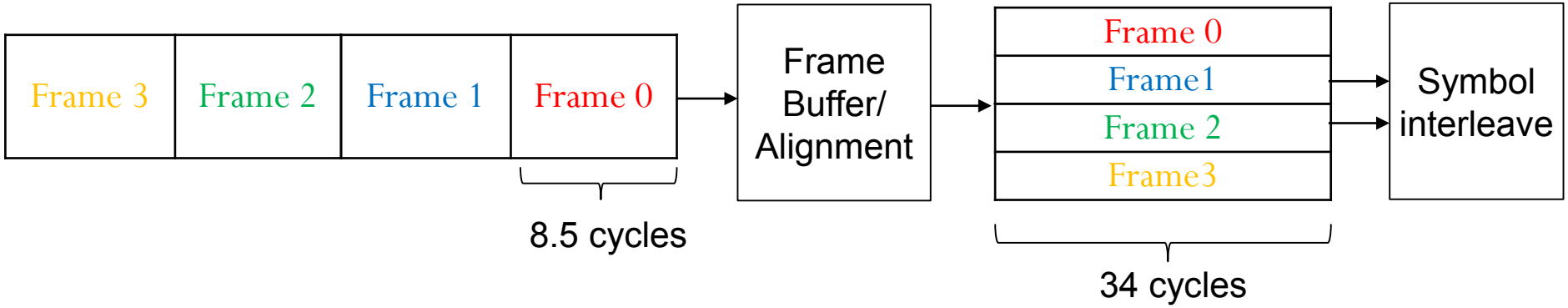
- **Scheme 6 in [2]**
- **For 4x100G FEC with 160 bit buswidth**:



- **Latency : 113ns.**
  - 3ns for encoder + 110ns for decoder
  - No extra latency for interleaving

4-way symbol interleaving

- **For 1x400G FEC with 640 bit buswidth**:
  - Symbol interleaved from 4 serial frames.

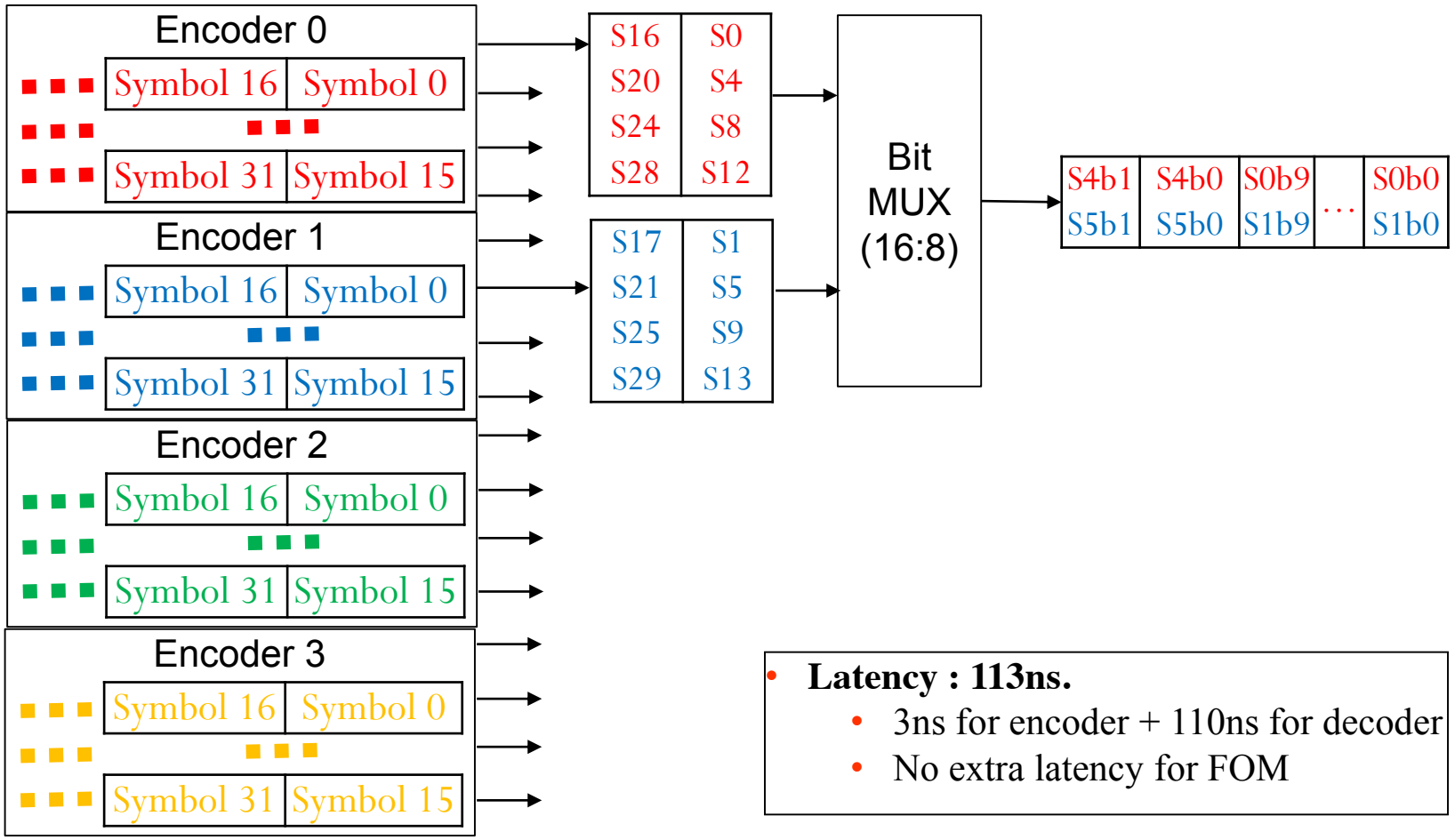


- **Latency:**
  - 8+17=25 extra cycles on both encoder and decoder sides to align frames
  - 75+37.5+37.5=150 ns.

- **Complexity**: ~9x5K bit extra memories
  - 4.5x5K memories on both encoder and decoder sides to buffer frames

FOM

- **Option 7 in [2]**
- **For 4x100G FEC with 160 bit buswidth**:



- **Latency : 113ns.**
  - 3ns for encoder + 110ns for decoder
  - No extra latency for FOM

Summary

- Latency for interleaving schemes with PMA Bit MUXing

Schemes / FEC	**1,2,3** No pre-interleave	**6** 4-way Interleaving	**7** FOM	**8** 2-way Interleaving
1x400G	**75ns**	150ns	-	99ns
2x200G	87ns	138ns	-	**87ns**
4x100G	113ns	**113ns**	**113ns**	113ns

- For schemes with 2:1 symbol MUX (2, 3, 9, and 10), a few cycles extra latency is needed for symbol MUXing
- Extra memories are needed if interleaved from serial frames.

Conclusions

- Without interleaving, the shortest latency is 75ns.
- For 2-way pre-interleaving, the shortest latency is **87ns**.
- For 4-way pre-interleaving, the shortest latency is 113ns.
- Coding gain difference between 2-way and 4-way pre-interleaving is small [2].