Electrical Interface Ad-hoc Report

IEEE P802.3bs 400Gb/s Ethernet Task Force

September 2015, Bonita Springs, FL

Electrical Ad Hoc Report

- The charter of the Electrical Interface Ad hoc is:
  - Address all issues in relation to the electrical interfaces to ensure progress towards a technically complete draft.
    - *Identify issues or omissions in the adopted Baselines*
    - *Find consensus now, rather than in comment resolution.*

- Next Ad-hoc Meeting
  - TBD, dates will be announced via the reflector

Electrical Interface Ad Hoc Presentations 11th Aug

Ad-hoc Opening/Agenda	Andre Szczepanek	szczepanek_01_081115_elect
Developments since CDAUI Baseline adoption	Andre Szczepanek	szczepanek_02_081115_elect
Simulations and Proposals For CDAUI8 link budgets	Magesh Valliappan and Raj Hegde	hegde_01_081115_elect

Electrical Interface Ad Hoc Presentations 24th Aug

Ad-hoc Opening/Agenda	Andre Szczepanek	szczepanek_01_082415_elect
CDAUI-8 Chip-to-Module (C2M) System Analysis	Stephane Dallaire Ben Smith	dallaire_01_082415_elect
CDAUI-8 PAM4 C2M Channel Investigations	Ed Frlan	frlan_01_082415_elect
C2M CDAUI-8: considerations towards first P802.3bs 400 Gb/s Ethernet draft	Marco Mazzini	mazzini_01_082415_elect
How a Linear filter could be added to COM based on Hegde_3bs_01_0715	Richard Mellitz	mellitz_01_082415_elect

Electrical Interface Ad Hoc Presentations 4th Sept

Ad-hoc Opening/Agenda/Closing	Andre Szczepanek	szczepanek_01_090415_elect
Options for CRU BW for 400GbE PAM4 PMDs*	Ali Ghiasi	ghiasi_01_082415_elect
120D/E TBD's in Draft 0.9		szczepanek_01_090415_elect
CDAUI-8 Chip-to-Module (C2M) System Analysis	Stephane Dallaire Ben Smith	dallaire_01_090415_elect
Discussion time		szczepanek_01_090415_elect

* Held-over from 24Aug Ad-hoc call

“TBD”s in Draft 0.9

Annex 120D (CDAUI-8 C2C)

- EEE support
- Receiver Jitter Tolerance
- Device package model:
  - Single-ended device capacitance
  - Single-ended board capacitance
- Single-ended termination resistance

Annex 120E (CDAUI-8 C2M)

- Transition time
- Host stressed input pattern generator jitter characteristics (Table 120E-5)
- Single-ended voltage tolerance range (min)
- Module stressed input Pattern generator jitter characteristics (Table 120E-8)