

Considerations for CRU BW 400 GbE PMDs in Support of Comments

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802.3bs Interim Meeting

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List of Contributors and Supporters

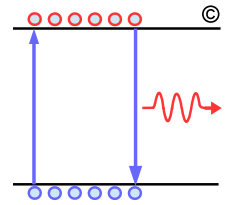
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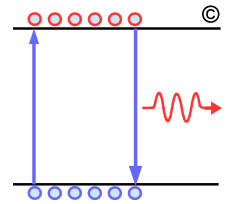
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Comments addressed



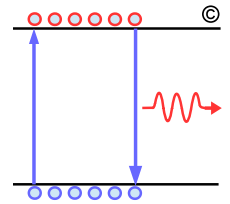
- Comment 93 CRU BW for 400Gbase-DR4
- Comment 94 stress receiver sensitivity for 400Gbase-DR4
- Comment 95 CRU BW for CDAUI-8
- Comment 96 stress receiver sensitivity for CDAUI-8
- Comment 103 CRU BW for CDAUI-8
- Comment 104 stress receiver sensitivity for CDAUI-8
- Comment 106 module stress receiver sensitivity for CDAUI-8
- Comment 109 output module CRU CDAUI-8
- Comment 110 Host stress sensitivity CDAUI-8
- Late comment CRU BW for 400Gbase-FR8/LR8
- Late comment stress receiver sensitivity for 400Gbase-FR8/LR8

Overview



- ❑ **Previously considerations for CRU and CDR BW have been presented in details**
 - http://www.ieee802.org/3/bm/public/mar14/ghiasi_01_0314_optx.pdf
 - http://www.ieee802.org/3/bs/public/15_07/ghiasi_3bs_01_0715.pdf
 - http://www.ieee802.org/3/ba/public/jan10/ghiasi_01_0110.pdf
- ❑ **802.3bs has no specific objective for a ports to be backward compatible with legacy 10 GbE, 40 GbE, or 100 GbE**
 - Since 802.3ae in Ethernet we have been using CRU BW of $F_{\text{baud}}/2578$
 - CRU BW for standards at 10.3125 GBd/lane is 4 MHz
 - CRU BW for standards at 25.78 GBd/lane is 10 MHz
 - The market however requires at least the host provide a level of backward compatibility
 - CDAUI-16 based on 4 instance of CAUI-4 carries forward 10 MHz CRU
- ❑ **Next will explore OSC/VCO phase noise and options for 802.3bs CRU BW.**

Consideration for CRU and CDR BW



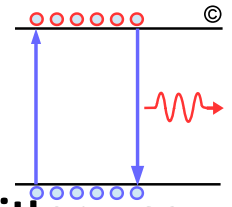
❑ Consideration for the golden PLL CRU BW

- Oscillator phase noise
 - Typical oscillator have flat phase noise > 1 MHz
- Crosstalk
 - High frequency effects >> CRU BW
- VCO phase noise
 - No benefit when CRU BW > 4MHz

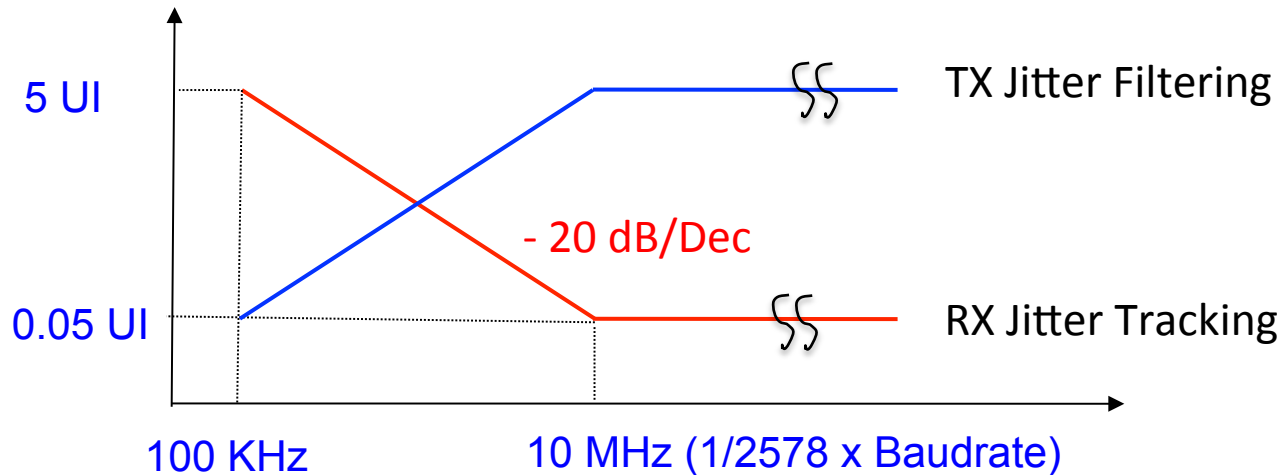
❑ Consideration for CDR BW

- Pattern dependent effect
 - Does not apply to 64B/66B/scrambled data with spectrum in the ~ 100 KHz
- Power
 - Higher loop BW results in higher CDR power
- DSP receiver
 - Timing recovery introduces latency making it challenging to meet traditional $F_{\text{baud}}/2578$ CDR loop BW
- Backward compatibility
 - Does an HOM port only operate at single speed with another HOM port or the port need to interoperate at lower bit rate with CAUI-4, CR4, SFI, etc?
 - An implementation requiring backward compatibility through a common data path would need 10 MHz CDR BW.

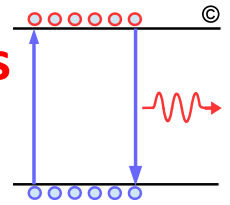
Comprehensive Jitter Methodology



- A comprehensive methodology to test transmitters and receivers for jitter was developed during 1 GFC standardization in the FC-MJS project and has become the basis for data communications system specification
- This methodology was based on systems using low cost oscillators and a reduction in power supply filtering to enable low-cost high-volume applications
 - Transmitter test assumes low frequency jitter should be tracked by a receiver, thus transmitter specs are relaxed by observing the transmitter using a reference PLL with OJTF defined as a high pass single pole filter with -20 dB/dec rolloff and -3dB corner frequency at 1/1667 Baudrate (changed to 1/2578*baudrate since 10 GbE)
 - Receiver test should complement transmitter test by verifying low frequency jitter is tolerated, example shown below is for a CRU/CDR response per CL 88.

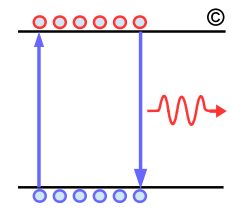


TX Jitter Filter and RX Jitter Tolerance for Several IEEE Standards



- ❑ **CL 52, 86A (40G-SR4, 100G-SR4), 83A/B (XLAUI, CAUI-10)**
 - Transmitter output measured with 4 MHz CRU (high pass jitter filter) $F_{\text{baud}}/2578$
 - Receiver is tested with worst case stress + TX credited low frequency SJ
- ❑ **CL 68 (LRM), CL 72 (10G-KR), CL 85 (40G-CR4/100G-CR10)**
 - Transmitter output measured with 4 MHz CRU (high pass jitter filter) $F_{\text{baud}}/2578$
 - CL 68 only tested unstress at two points (75 KHz, 5 UI) and (375 KHz, 1 UI)
 - CL 72 interference test require testing receiver with 0.115 UI at $F_{\text{baud}}/250$
 - CL 85 interference test require testing receiver with 0.115 UI at frequency > 15 MHz
- ❑ **CL 88 (100G-LR4), CL 95 (100G-SR4), CL83D/E (CAUI-4)**
 - Transmitter output measured with 10 MHz CRU (high pass jitter filter) $F_{\text{baud}}/2578$
 - Receiver is tested with worst case stress + TX credited low frequency SJ
- ❑ **CL 92 (100G-CR4), CL 93 (100G-KR4)**
 - Transmitter output measured with 10 MHz CRU (high pass jitter filter) $F_{\text{baud}}/2578$
 - CL 92 interference test require testing receiver with 0.1 UI at frequency > 100 MHz and unstress SJ testing at (190 KHz, 5 UI) and (940 KHz, 1 UI)
 - CL 93 tested with 35 dB ISI channel at (190 KHz, 5 UI) and (940 KHz, 1 UI)
- ❑ **CL 94 (100G-KP4)**
 - Transmitter output measured with a CRU having 20 dB/dec low frequency response, 1.6 MHz BW, and 3 dB peaking at 6 MHz, response has peaking to accommodate 2nd order loops and potential peaking as result of DSP timing recovery latency
 - Receiver is tested unstress with following SJ components (16 KHz, 5 UI) and (160 KHz, 0.5 UI), jitter tolerance actually does not reflect the intention of 2nd order CRU
- ❑ **10G-LRM and 100G-KP4 tests receivers unstress may not guarantee interoperability**
 - 10G-KR and 40G-CR4/100G-CR10 interference tolerance does have an SJ component but does not test against test full range of SJ allowed by the transmitter.

Transmitter Jitter Filter vs Receiver Jitter Tracking for Several IEEE Standards



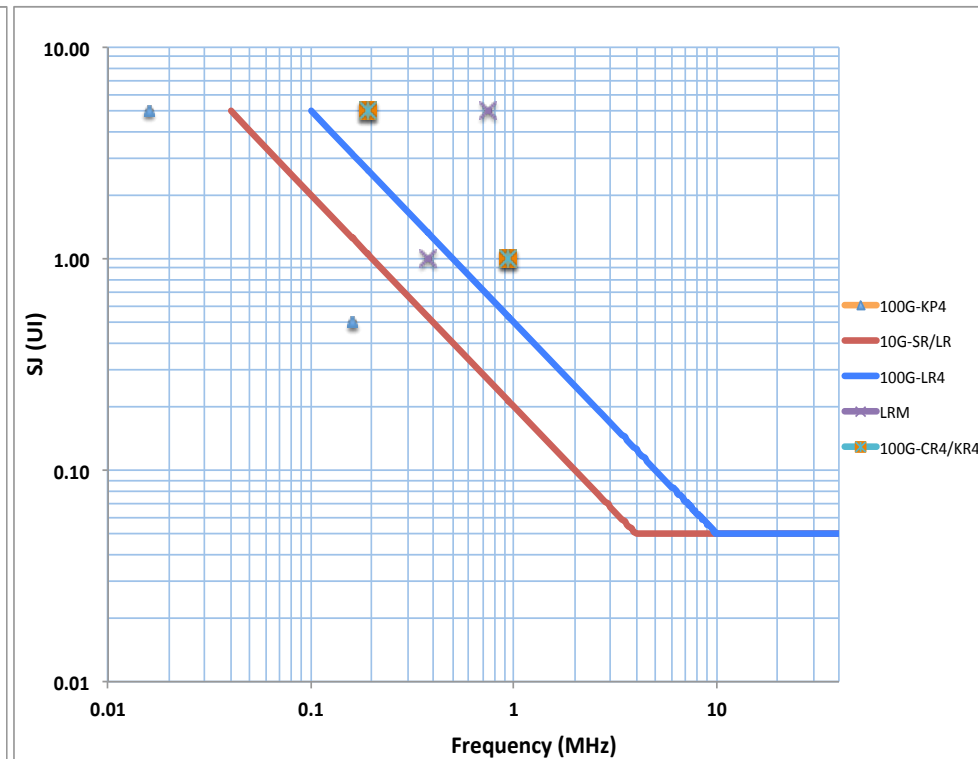
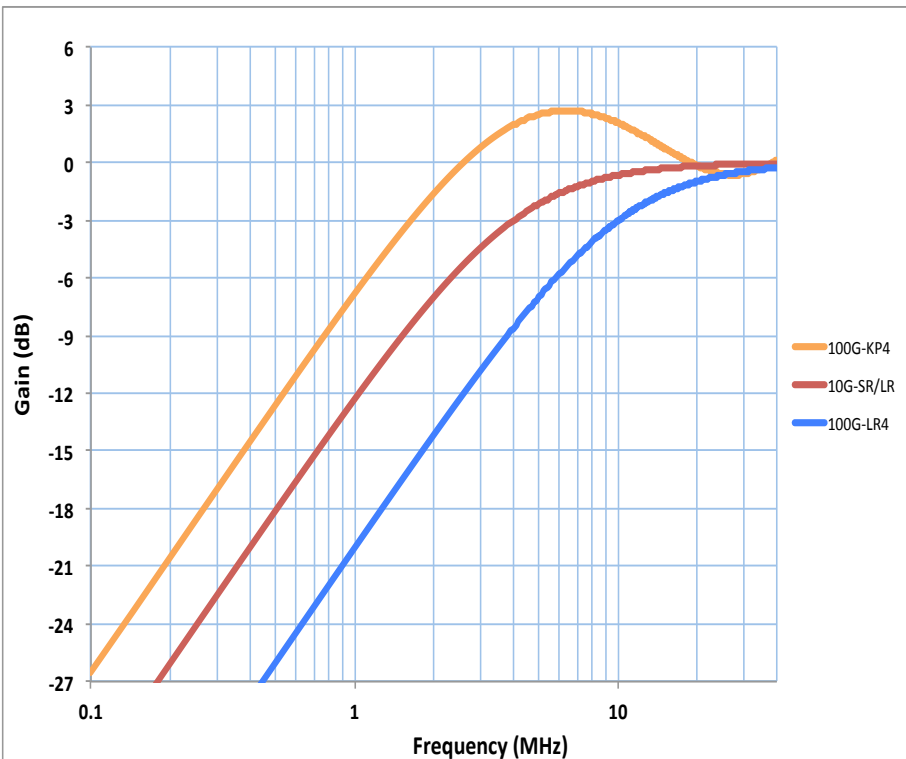
- The receiver must track the low frequency jitter golden PLL filters for observation on the scope, only 100G-KP4 defines higher than 1st order response as defined by:

$$G(f) = \frac{f}{f - j \times f_n e^{(j2\pi fT)}} , \text{ where } f_n = 2.12 \text{ MHz and } T = 0.0286 \mu\text{s}$$

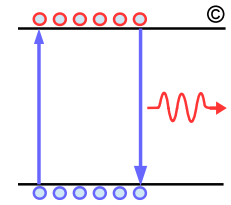
- CRU with 3 dB is not an option for pass-through links due to cascaded effect of jitter peaking.

Golden PLL “TX Jitter Filter” Response

Stress Sensitivity

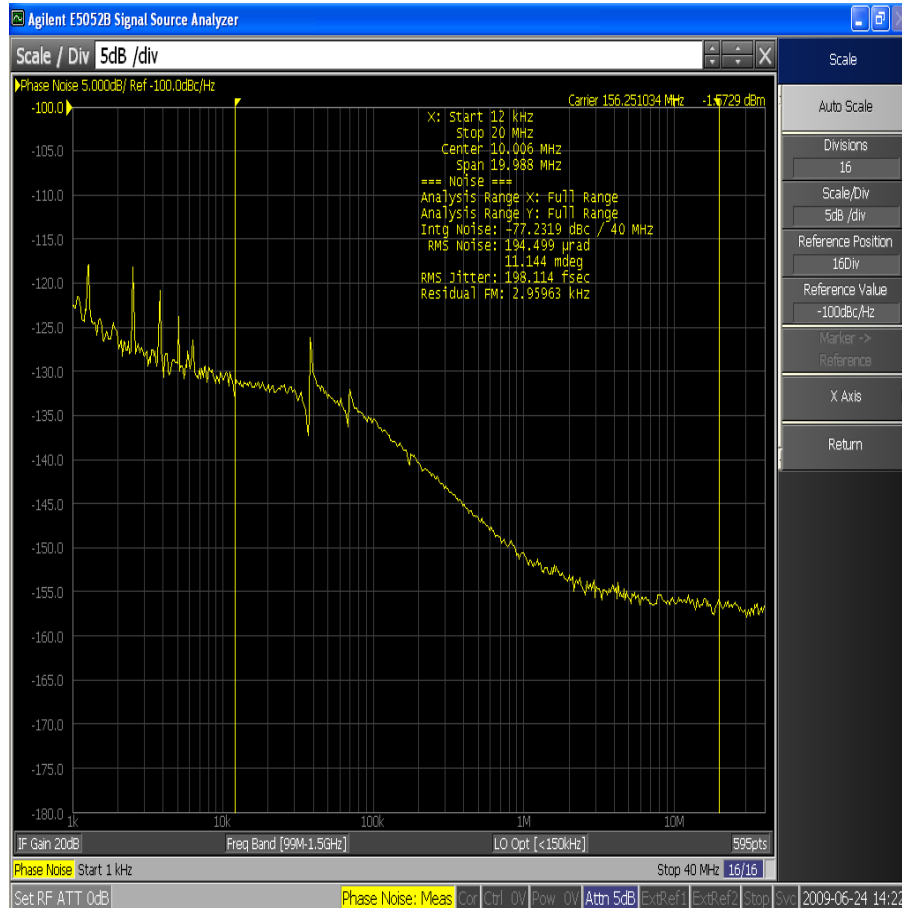


Typical Low Cost Oscillator Phase Noise Plot (from ghiasi_01_0110.pdf)

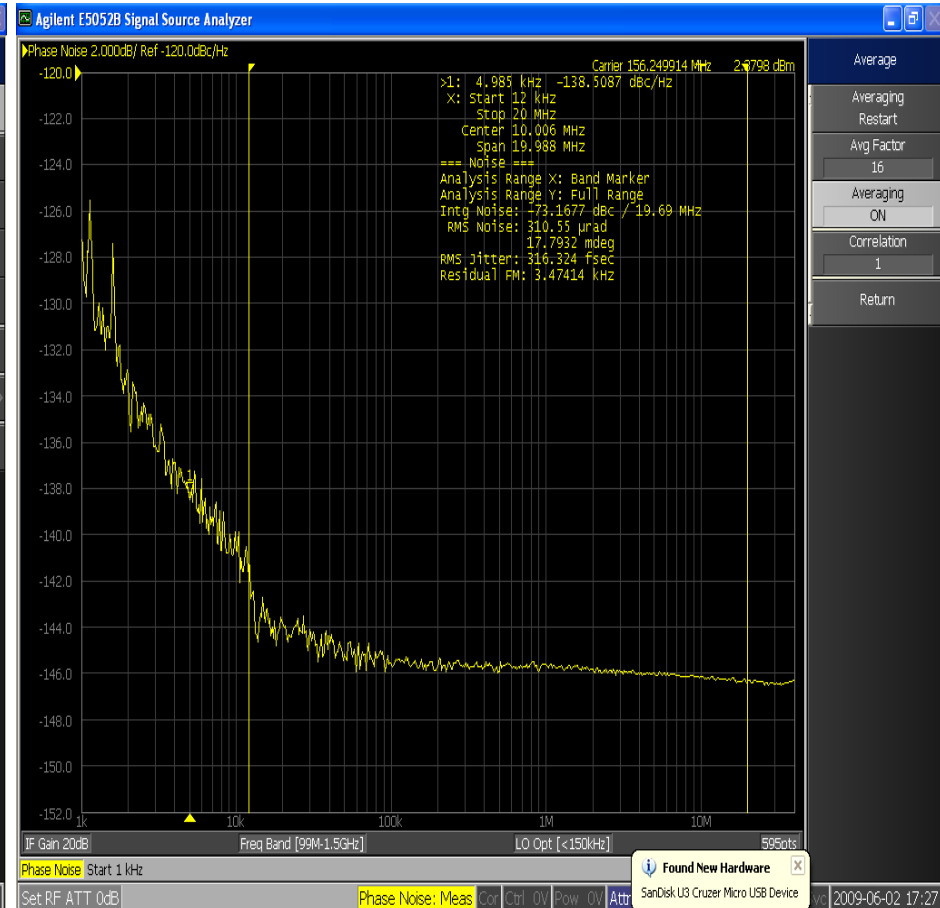


- Considering two very different oscillator 4 MHz CDR loop BW is a good compromise!

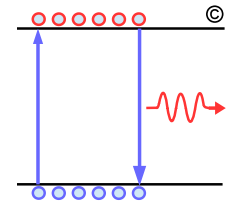
OSC-I



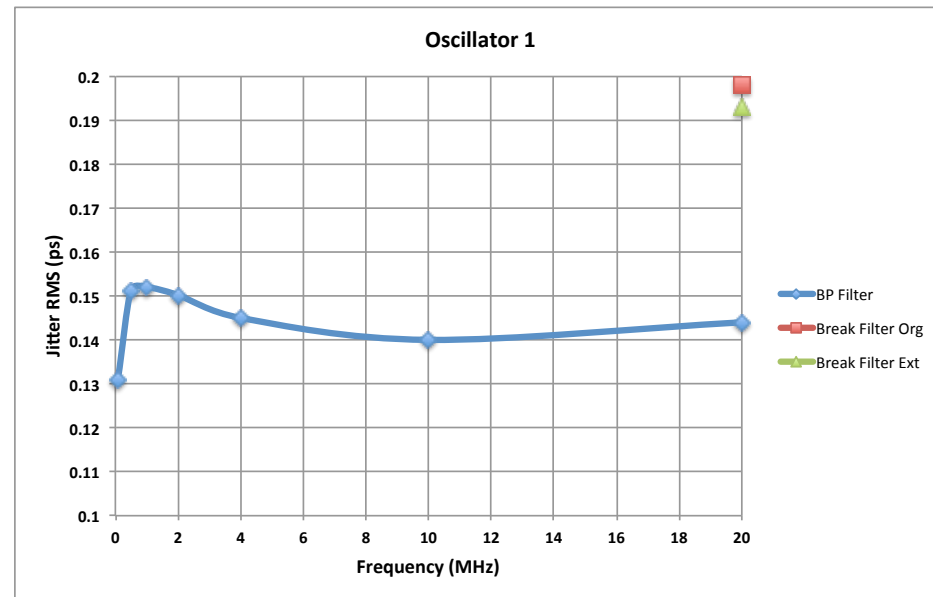
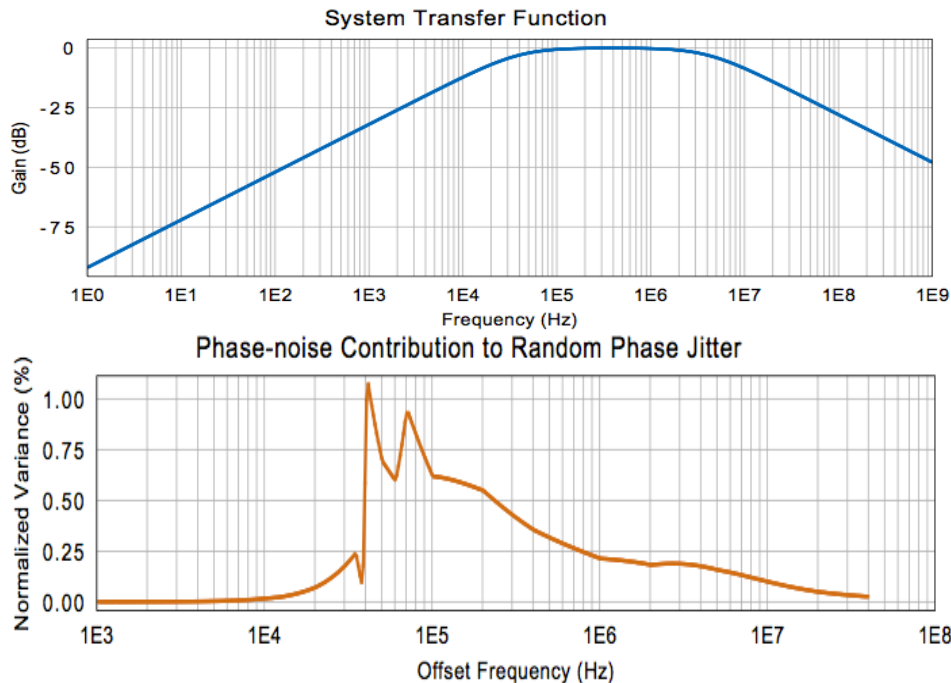
OSC-II



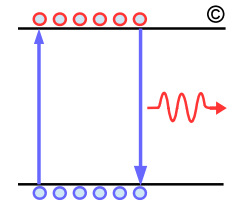
Analysis of Oscillator I



- Readout from oscillator graph were entered into <https://www.jitterlabs.com/support/calculators/> to analysis the oscillator integrated phase noise for band pass response
 - Result shown below are for 4 MHz low pass response with high pass pole at 1/100 of low pass pole
 - Integrated phase noise calculated for band pass response by varying LP pole form 0.1-20 MHz
 - Phase noise analyzer reported RMS jitter for break filter of 12 KHz-20 MHz and the data point is shown on the graph and compared to the calculated result for match.

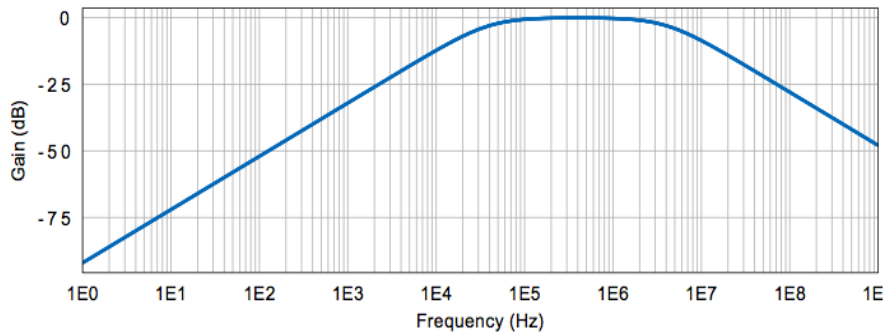


Analysis of Oscillator II

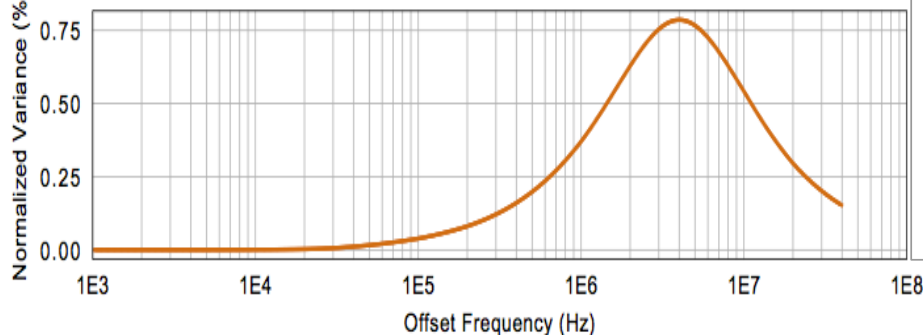


- Readout from oscillator graph were entered into <https://www.jitterlabs.com/support/calculators/> to analysis the oscillator integrated phase noise for band pass response
 - Result shown below are for 4 MHz low pass response with high pass pole at 1/100 of low pass pole
 - Integrated phase noise calculated for band pass response by varying LP pole form 0.1-20 MHz
 - Phase noise analyzer reported RMS jitter for break filter of 12 KHz-20 MHz and the data point is shown on the graph and compared to the calculated result for match.

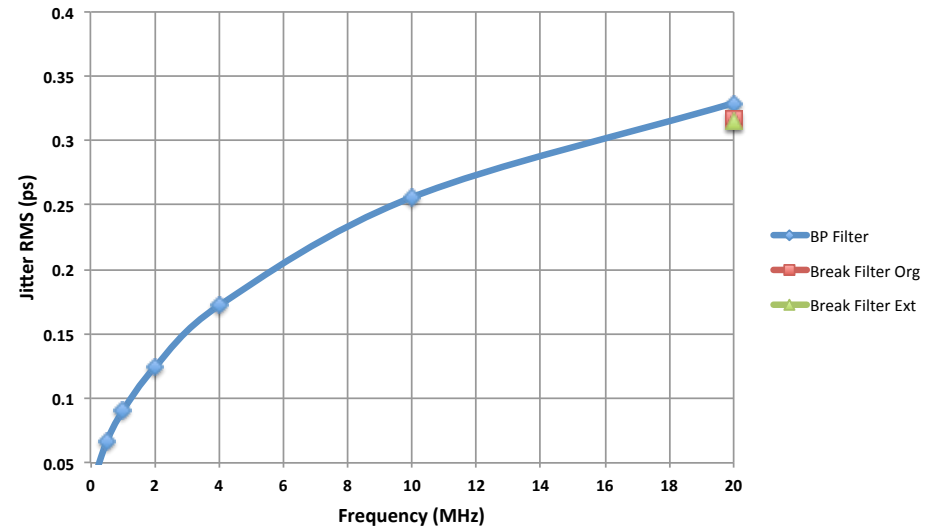
System Transfer Function



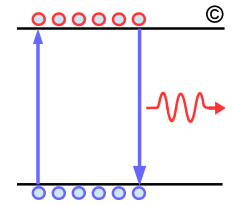
Phase-noise Contribution to Random Phase Jitter



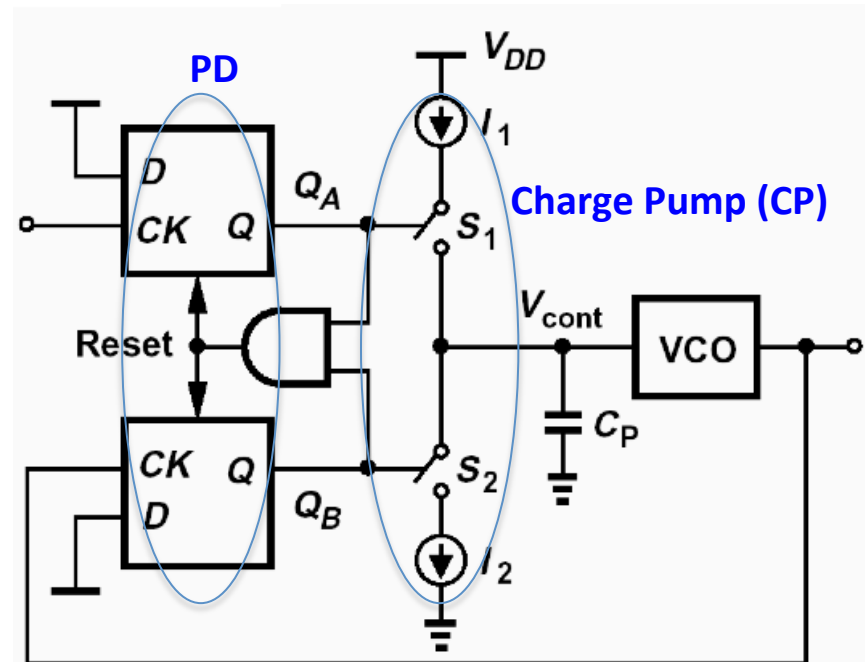
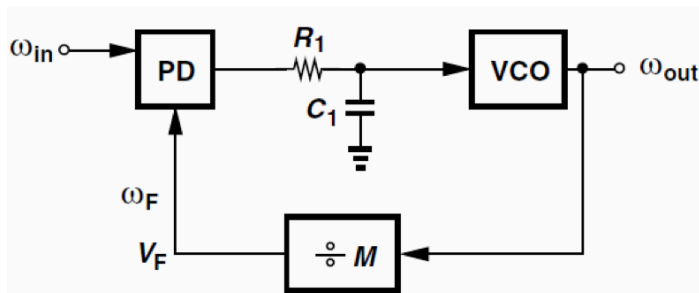
Oscillator 2



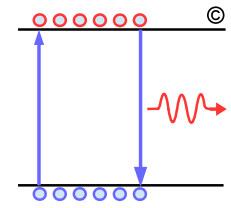
Basic PLL Structures



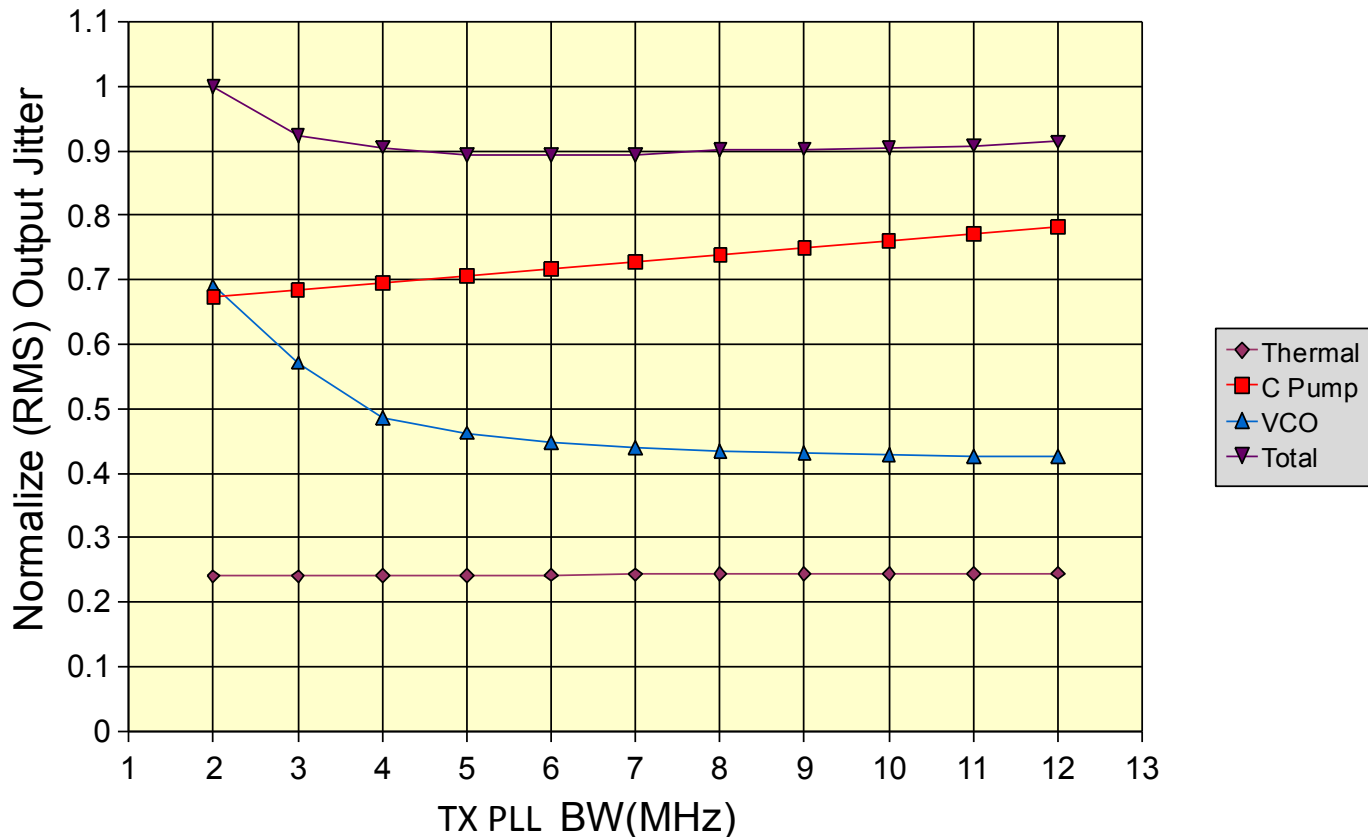
- ❑ PLL structures used for noise analysis include charge pump with better capture range and phase error
- ❑ Basic PLL structure and PLL structure with charge pump as illustrated by following lecture Behzad Razavi (UCLA)
 - See http://www.seas.ucla.edu/brweb/teaching/215C_W2013/PLLs.pdf
 - PLL filter also acts as filter for charge pump and increasing filter BW increases CP noise.



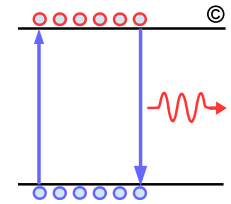
SerDes Transmitter Relative Jitter (from ghiasi_01_0110.pdf)



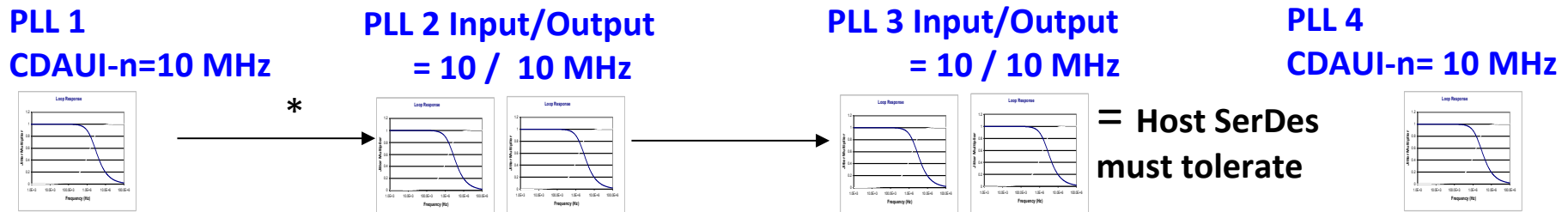
- Thermal, charge pump, VCO, and total relative output jitter as function of BW
 - VCO phase noise has limited benefit for BW > 4MHz
 - Charge pump noise a dominant noise source increases with increase in BW
 - Result below excludes OSC noise but 4 MHz is a good compromise considering OSC-I/OSC-II.



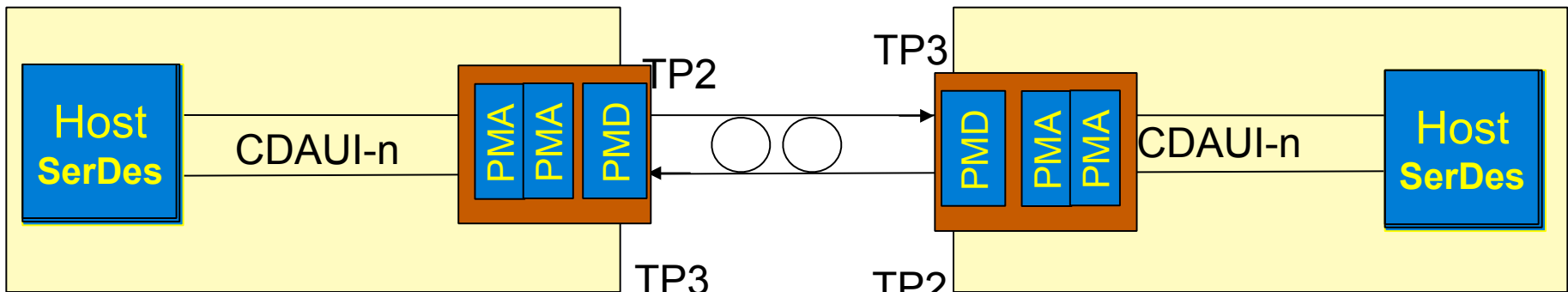
Option I: Assume 10 MHz CRU BW



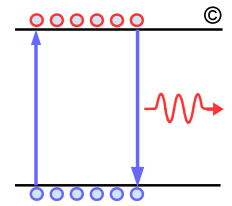
- ❑ Propose to use 10 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8
- ❑ It simplifies the overall architecture at expense of requiring faster tracking BW resulting in higher power on more complex PAM4 receivers
 - This approach is backward compatible with previous IEEE standards and compatible with CDAUI-16 which is based on CAUI-4
 - Allow implementation to follow current 100G retimer modules based on CAUI-4 based on simple CDR without FIFO (insertion/deletion or phase) when PMA device number of in/out lanes are equal.



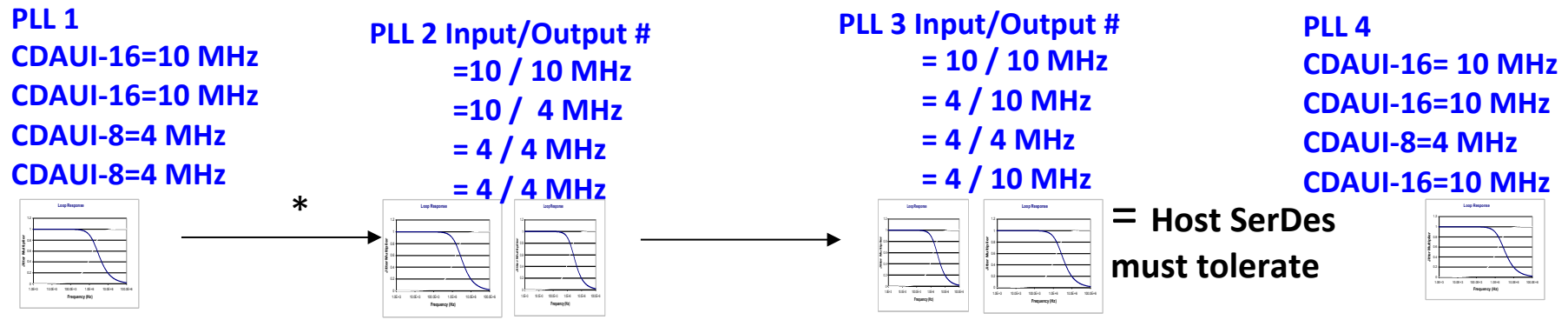
* Forward propagation illustrated reverse propagation would be similar.



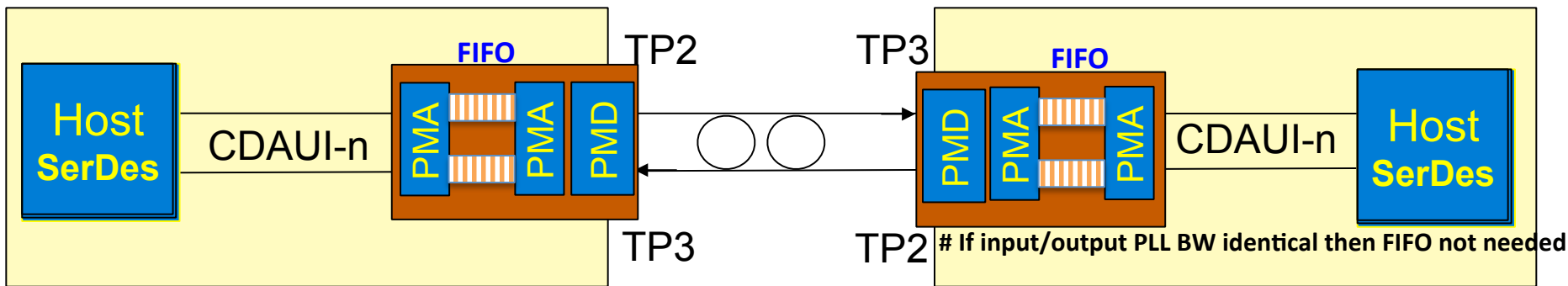
Option II: Assume 4 MHz CRU BW



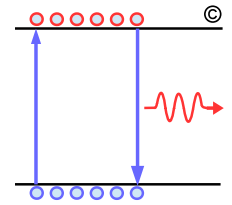
- Propose to use 4 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8
 - Backward compatible with 10.3125 GBd/lane PMD's
 - 4 MHz tracking BW could benefit more complex PAM4 Cu/MMF receivers and reduce power
- This approach is not fully backward compatible with IEEE standards operating 25.78 GBd/lane or CDAUI-16 which is based on CAUI-4 having 10 MHz CRU BW, but can be managed as following:
 - Module PMA does not need FIFO in case of CDAUI-8 host in conjunction with 8 lanes PMDs
 - CDAUI-8 host operating with legacy host based on 25.78 GBd/lane require a PMA-PMA chip with FIFO and/or dual loop PLL
 - Anytime number of in/output lanes are not equal to manage differential skew FIFO is required anyway
 - For improve compatibility wander on CAUI-4 should be limited to 5 UI from 40 kHz-100 kHz.



* Forward propagation illustrated reverse propagation would be similar.



Option IIA: Assume 4 MHz CRU BW



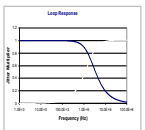
- Propose to use 4 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8
 - Backward compatible with 10.3125 GBd/lane PMD's
 - 4 MHz tracking BW could benefit more complex PAM4 Cu/MMF receivers and reduce power
- This approach is not fully backward compatible with IEEE standards operating 25.78 GBd/lane based on CAUI-4 having 10 MHz CRU BW:
 - The assumption is that most CAUI-4 SerDes core today have enough margin to meet CDAUI-16 TX jitter with 4 MHz CRU
 - A 4 MHz common CRU BW for both CDAUI-16 and CDAUI-8 simplifies the architecture and allow simple PMA implementation without the need for deep parallel FIFO

PLL 1
CDAUI-16=4 MHz

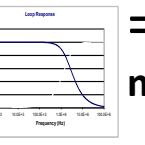
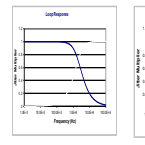
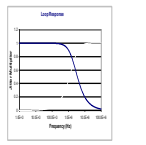
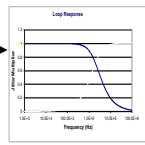
PLL 2 Input/Output #
=4 / 4 MHz

PLL 3 Input/Output #
= 4 / 4 MHz

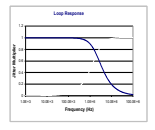
PLL 4
CDAUI-16= 4 MHz



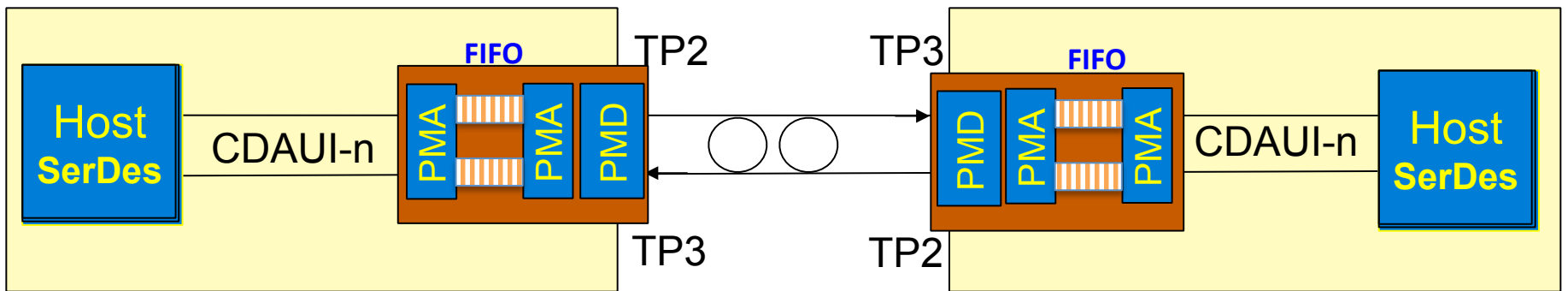
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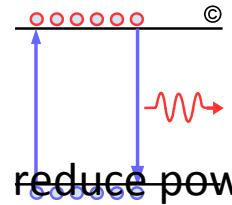
= Host SerDes must tolerate



* Forward propagation illustrated reverse propagation would be similar.



Option III: Assume 2 MHz CRU BW



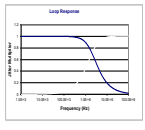
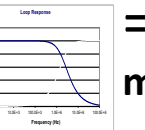
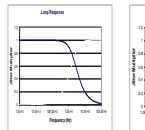
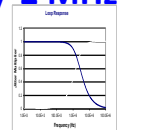
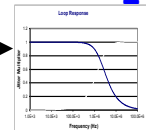
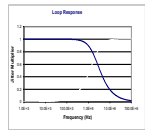
- Propose to use 4 MHz CRU BW for CDAUI-8, 400Gbase-DR4, 400Gbase-FR8/LR8
 - 2 MHz tracking BW benefits more complex PAM4 Cu/MMF receivers and reduce power
- This approach is not backward 10 GbE (4 MHz CRU) nor to 25.78 GBd/lane (10 MHz CRU) and need to manage jitter transfer as following:
 - Module PMA does not need FIFO in case of CDAUI-8 host in conjunction with 8 lanes PMDs assuming CDAUI-8 has the same CRU BW
 - CDAUI-8 host operating with legacy host based on 25.78 GBd/lane require a PMA-PMA chip with FIFO and/or dual loop PLL
 - Anytime number of in/output lanes are not equal to manage differential skew FIFO is required anyway

PLL 1
 CDAUI-16=10 MHz
 CDAUI-16=10 MHz
 CDAUI-8=2 MHz
 CDAUI-8=2 MHz

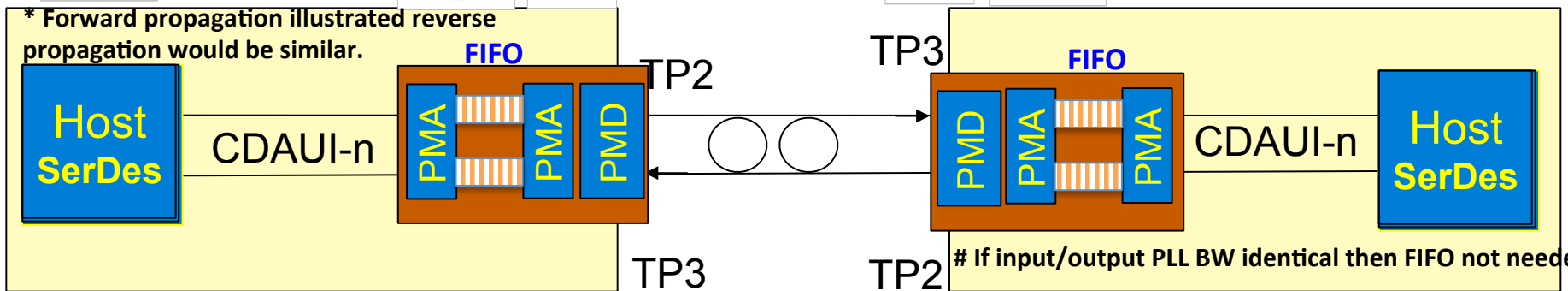
PLL 2 Input/Output #
 =10 / 10 MHz
 =10 / 2 MHz
 = 2 / 2 MHz
 = 2 / 2 MHz

PLL 3 Input/Output #
 = 10 / 10 MHz
 = 2 / 10 MHz
 = 2 / 2 MHz
 = 2 / 10 MHz

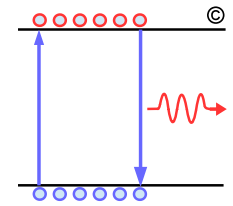
PLL 4
 CDAUI-16= 10 MHz
 CDAUI-16=10 MHz
 CDAUI-8=2 MHz
 CDAUI-16=10 MHz



= Host SerDes must tolerate

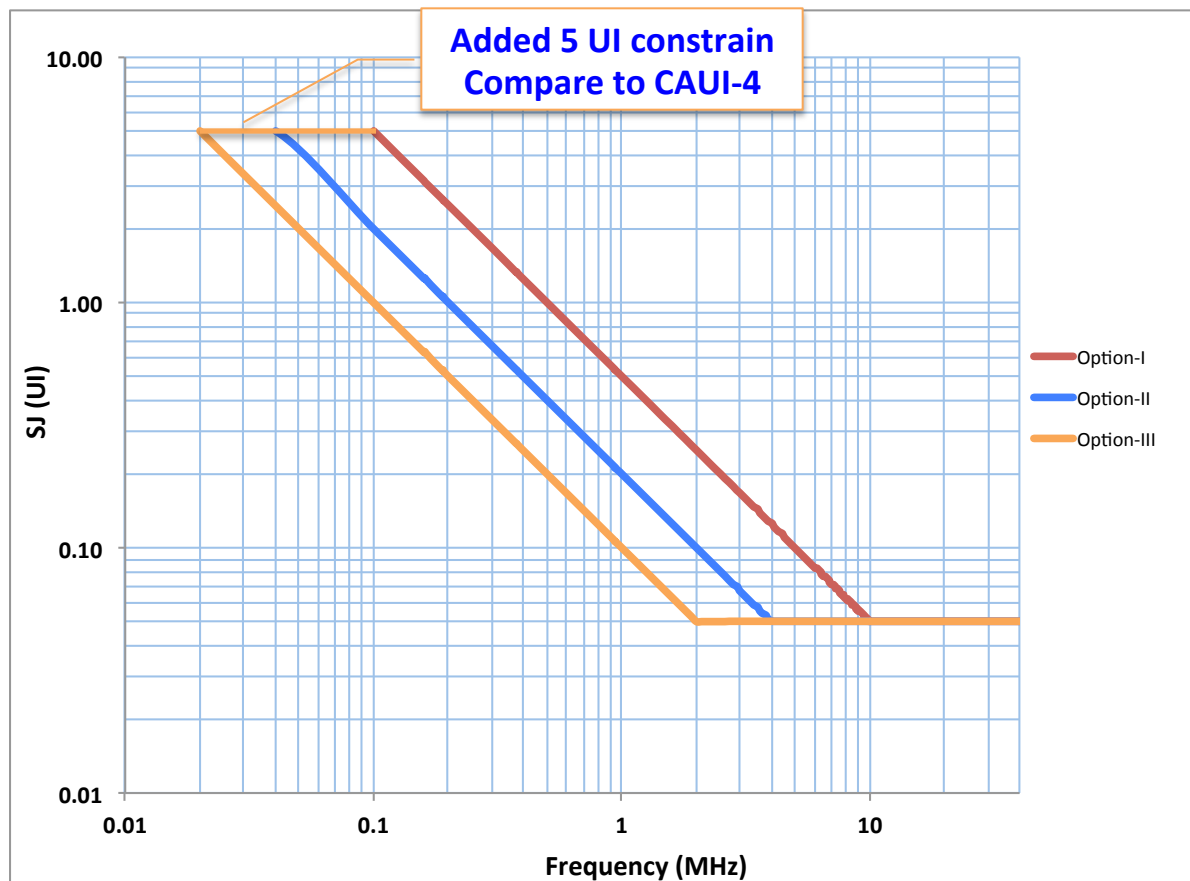


Wander from 40 kHz-100 KHz should be Constrained

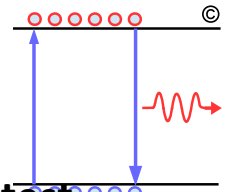


□ CAUI-4 10 MHz CRU does not define wander from 20 KHz or 40 kHz to 100 kHz

- Suggest to constrain CDAUI-16 max wander generation to 5 UI
- Option IIA is identical to option II except it does not require adding 5 UI constrain.



Summary



- ❑ **Reliable link operation requires that the receiver test complements transmitter test**
 - Golden CRU having high pass response mask the transmitter low frequency jitter components propagating down the link that the receiver must tolerate
- ❑ **HOM receivers are more complex with timing recovery potentially having higher latency could make it difficult to support $F_{\text{baud}}/2578$ CRU**
 - CDAUI-16 based on CAUI-4 forces 10 MHz CRU into the 802.3bs
 - Adding 5 UI wander generation from 40-100 KHz on CDAUI-16 ports will simplify implementation of CDAUI-8-CDAUI-16 without the need for insertion-deletion FIFO
 - If input/output lanes are not equal or at termination SerDes FIFO is required to absorb dynamic skew and could also be designed to absorb 10 MHz CRU jitter
- ❑ **Three viable options explored are:**
 - Option I: 10 MHz CRU BW for all 50/100 Gb/s PAM4 PMDs allow full backward compatibility with CDAUI-16 as well as legacy PMD support but at expense of power and possibly limiting the implementation
 - Option II/III: 4 MHz/2 MHz CRU BW for all 50/100 Gb/s PAM4 PMDs with low frequency wander constrain the CDAUI-16 ports to eliminates the need for insertion/deletion FIFO and provide backward compatibility
 - PAM4 PMAs interoperating with legacy NRZ PMDs with open eye likely will have full tracking BW
 - Option IIA where CDAUI-16 and CDAUI-8 both have common 4 MHz CRU BW can simplify the PMA implementation
- ❑ **10 MHz CRU BW is challenging considering future more complex HOM PMDs but we know how to deal and manage any interoperability issue choosing 4 or 2 MHz CRU**
- ❑ **What ever we choose for CRU BW the receiver must operate with identical stress and be able to tolerate jitter components masked by the transmit CRU high pass response.**