

# TX LINEARITY MEASUREMENT PROPOSAL

(IN SUPPORT OF COMMENT #118)



**Magesh Valliappan & Raj Hegde**  
IEEE 802.3bs 400Gb/s Task Force  
Atlanta, January, 2016

- **Overview of CDAUI-8 c2c TX linearity Specifications in Draft 1.1**
- **Proposal to change usage of  $R_{LM}$  & SNDR**
- **Proposal to change method to measure PAM4 TX levels**

- Inherited from Clause 94 (100GBase-KP4) and referenced by TX SNDR &  $R_{LM}$ 
  - 94.3.12.5.1 Transmitter linearity
    - Measure TX Linearity Test Pattern to obtain  $V_A$ ,  $V_B$ ,  $V_C$ ,  $V_D$
    - Calculate **ES<sub>1</sub>** & **ES<sub>2</sub>** (to allow for asymmetric inner PAM4 data levels) and  $R_{LM}$

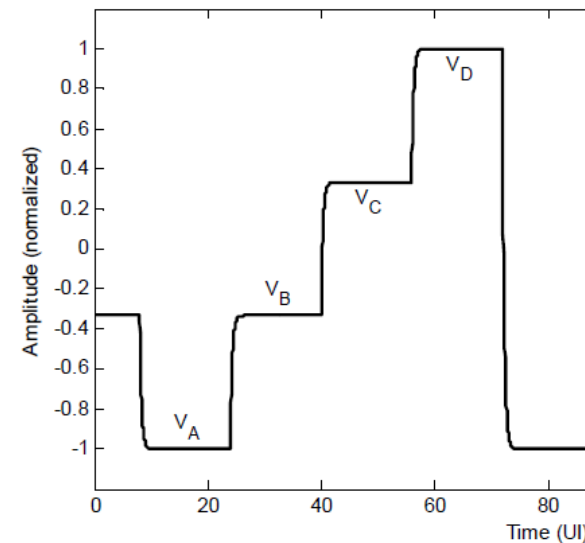
$$S_{\min} = \frac{\min(V_D - V_C, V_C - V_B, V_B - V_A)}{2}$$

$$V_{\text{avg}} = \frac{V_A + V_B + V_C + V_D}{4}$$

$$ES_1 = \frac{V_B - V_{\text{avg}}}{V_A - V_{\text{avg}}}$$

$$ES_2 = \frac{V_C - V_{\text{avg}}}{V_D - V_{\text{avg}}}$$

$$R_{LM} = \frac{6 \cdot S_{\min}}{V_D - V_A}$$



- 94.3.12.5.2 Linear fit to the measured waveform
  - Measure PRBS13Q
  - Calculate **SNDR**, **p(k)** using an assumption that data levels are  $(-1, -ES_1, ES_2, 1)$

- $R_{LM}$  constraint on the TX should provide reasonable implementation margin for TX while limiting impact on the RX complexity and link budget
- Current  $R_{LM}$  specification is based on the minimum eye opening between the 4 PAM levels
- PAM4 levels are  $[-1, -ES1, +ES2, +1]$  with  $ES1=ES2=1/3$  in the normal case
  - Current  $R_{LM}$  spec allows these TX cases with no downside or penalties

% error on ES1 & ES2	Notes
-5%, -5%	Symmetric case with 5% smaller middle eye
+10%,+10%	Symmetric case with 5% smaller outer eyes (compressed outer levels)
-20%,+10%	Asymmetric case with 10% larger lower eye and 5% smaller upper eye
+10%,-20%	Asymmetric case with 5% smaller lower eye and 10% larger upper eye

- For a 1Vpp example, the asymmetric cases have voltage levels of  $[-500, -133, +183, +500]$  mV
- The difference between the  $+1/3$  and  $-1/3$  levels is 50mV

- **Transmitters designed for electrical links have good vertical symmetry (ES1  $\approx$  ES2)**
  - CAUI4, 100G-CR4 & 100G-KR4 constrain vertical asymmetry by SNDR. We can do the same here.
- **Current spec allows large deviations from ideal levels (up to 20% in asymmetric case)**
  - COM models the reduction in ideal eye opening implied by  $R_{LM}$ , but assumes perfect ISI cancellation by DFE
  - It is not practical for a DFE to achieve this when TX levels are distorted
  - Margin impact is proportional to the max. error on ES1 and ES2 and DFE tap weights
  - Need to constrain the maximum error on ES1 and ES2 to avoid the worst case effect
  - Assume that 5% errors in ES1 and ES2 can be absorbed by RX implementation budgets
- **$R_{LM}$  spec allows larger deviation (+10%) on the positive side of ES1 and ES2**
  - In addition to DFE's imperfect ISI cancellation, this case is further aggravated by RX circuit compression
  - Even with perfect linearity in the RX, PAM4 outer eyes are already more distorted.
- **With the proposed best fit method to estimate ES1 & ES2 accurately, there is less concern about measurement errors**

- **Estimate ES1 & ES2 using best fit method**
- **$R_{LM}$  defined to capture maximum deviation from ideal**
  - $R_{LM} = \text{Min}(3*ES1, 3*ES2, 2-3*ES1, 2-3*ES2)$  with limit of 0.95
  - This will allow ES1 and ES2 to assume values of +/- 5% around ideal value of 1/3
- **Define  $ES = (ES1 + ES2)/2$**
- **Change SNDR to use the source TX levels as [-1, -ES,+ES,+1]**
- **+/-5 % error in TX levels should be absorbed by RX implementation, but recommend 3dB COM margin**
- **Advantages**
  - **No impact to common TX cases** with symmetric levels within +/-5% of ideal
  - SNDR now captures symmetry errors
    - Low levels of vertical asymmetry do not affect SNDR measurably
      - $ES1, ES2 = (+2\%, -2\%)$  results in < 0.1dB SNDR penalty