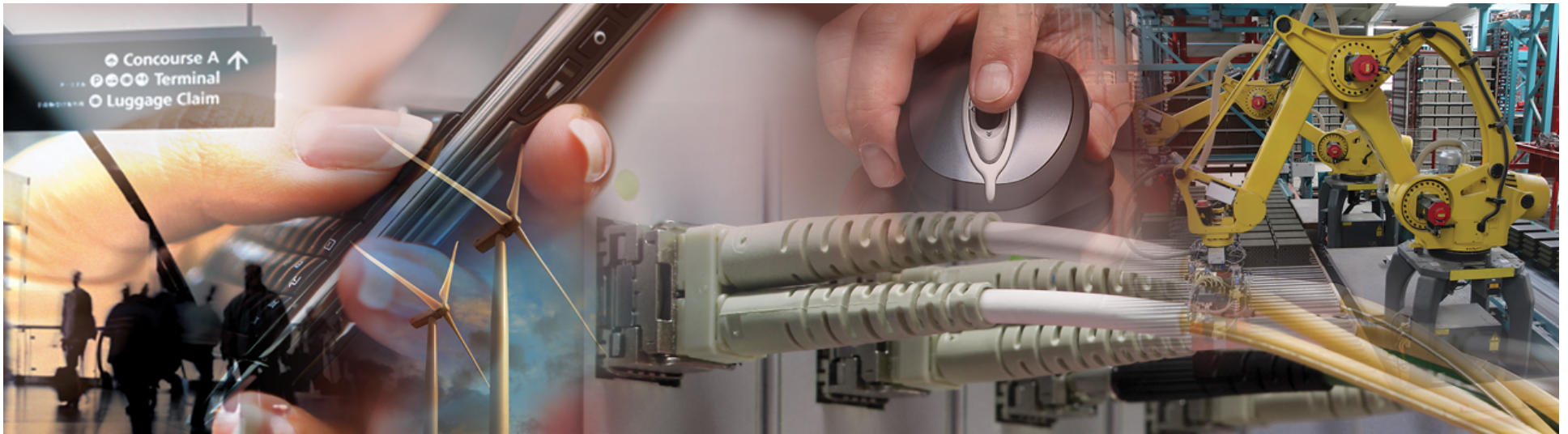


# Supporting materials for comment #47



**Jeff Slavick**

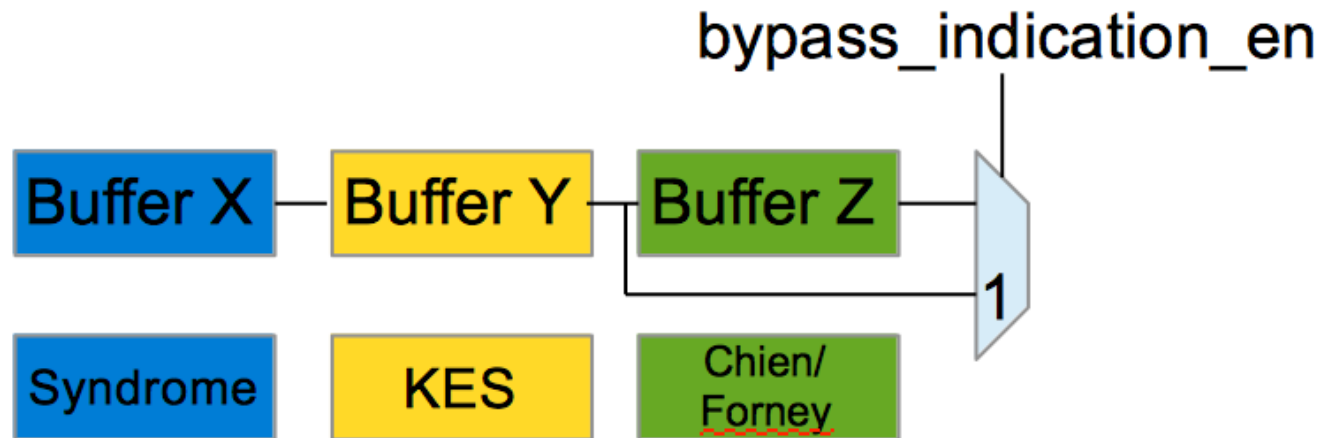
# Supporters

**CI 119**      **SC 119.2.5.3**                      **P 97**                      **L 28**                      # **47**  
Slavick, Jeff    Avago Technologies

*Comment Type*      **T**                      *Comment Status*      **X**

Bypass error indication feature is not included. This is a very useful feature to enable the user to reduce latency (~25% of the FEC latency). When a link can run with an uncorrected error rate of 0 you can reduce latency by turning off the error indication feature. When segments in the link aren't running at the specified limits then an uncorrected error rate near 0 can be achieved. Designs supporting 25GE and 100GE RS-FEC designs (which include this feature) would likely support it for 400G as well, so adding the specification ensures the appropriate check is done to ensure MTTFPA. Correction of the FEC codewords still occurs, the FEC skips buffering the data to validate that the codeword was completely fixed before passing it onto the PCS decoder. It's safe to bypass this buffering since you're non-fixable error rate (uncorretable errors) is 0. This feature would be usable before bypass\_correction is usable, and bypass correction is currently part of the RS-FEC's definition.

# Error indication bypass does what?



- With error indication on the latency through the FEC decoder is  $X + Y + Z$
- With bypass error indication on you save  $Z$  amount of latency
- For 400G
  - $X \sim 25\text{ns}$  ( $5440 \cdot 2 / 26.5625$ )
  - $Y < 50\text{ns}$
  - $Z < 25\text{ns}$  (tradeoff of area versus latency)

# RS-FEC operating modes in standards

Mode	Description	BJ	BY	BS
All on	All features enabled, Best MTTFPA	X	X	X
Bypass Indication	CW corrected, data released to PCS before validation all errors were corrected, MTTFPA protected by checking BER rate is sufficiently “good” for uncorrectable errors to be effectively be 0	X	X	? <sup>1</sup>
Detect Only	RS-FEC transmitted, receiver just checks for 0 errors, when errors present all data in CW is marked bad, requires input BER to be effectively 0 to use	X	X	X <sup>2</sup>
RS-FEC Bypass <sup>3</sup>	RS-FEC is bypassed and raw 64b66b data is sent		X	

1. Comment #49 against D1.1 requests to add this feature in
2. Comment #128 against D1.1 requests to remove this feature
3. Needed since BY negotiates use of RS-FEC for PHYs with CI108, while BJ & BS require RS-FEC transmission

# RS-FEC Latency versus required BER

Mode	400G Latency	400G Max BER
All on	~100ns	2.4e-4
Bypass Indication	~75ns	~3e-5
Detect Only	~25ns	~5e-14
RS-FEC Bypass	N/A	N/A

Assumption is that X=Y=Z from slide 2.

# MTTFPA protection<sup>1</sup>

- **All On mode**
  - Watch for consecutive uncorrectable codewords in a row and take the link down when that occurs
- **Bypass Indication**
  - There should be no uncorrectable codewords, but need to watch for them. So additional monitoring of SER (RS-symbol error rate) is done to take the link down if it degrades to a point where MTTFPA is a concern (uncorrectable codewords probability is too high).
- **Detect Only**
  - Any error causes data to be thrown away, so no MTTFPA concern

1. See [http://www.ieee802.org/3/bs/public/adhoc/logic/dec11\\_15/sun\\_01\\_1215\\_logic.pdf](http://www.ieee802.org/3/bs/public/adhoc/logic/dec11_15/sun_01_1215_logic.pdf) for additional details on MTTFPA protection thresholds

# Why add bypass indication

- **Other PHY types**
  - Designs supporting multi-rate will have this feature for the “others”
  - Designs supporting multi-rate will likely add this feature for 400G even if it’s non-standard
- **Only requires a small improvement in link performance from the worst-case**
  - As technology improves, links will not be running at the specification limits and BER will quickly reach levels this feature is usable at
- **Latency savings**
  - While 25ns isn’t a lot for optical links, copper is likely to come in the future and it would matter then.
  - Many systems require 0 uncorrectable error blocks for operation (no lost packets), why not enable latency savings for those systems



# Conclusion

- **Add the bypass indication feature**
  - It'll show up in designs anyways, previous gen PHY types have it
  - It's usable with a mild link error rate improvement
  - Future proof the standard since this feature will likely be added when copper PHYs comes along
    - if 200G includes copper and uses CI119 RS-FEC could be sooner then later