CDAUI-8 Chip-to-chip Jitter Budget Proposal

In support of Comment # 149

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Motivation

- Current specification in Table 120D-1

Jitter Type	Amount
CRJ max (RMS)	0.01 UI
CDJ max (pk-pk)	0.04 UI
Even-odd max	0.019 UI

- Measurement method employed is specified in 94.3.12.6
  - For CRJ and CDJ:
    - JP03A test pattern – repeating {0, 3} sequence
    - Extraction using J_5 and J_6

$$\begin{bmatrix} CRJrms \\ CDJ \end{bmatrix} = \begin{bmatrix} 1.0538 & -1.0538 \\ -9.3098 & 10.3098 \end{bmatrix} \begin{bmatrix} J_6 \\ J_5 \end{bmatrix}$$

- Extrapolation from J_5 and J_6 is not reliable
  - Concerns raised in [healey_3bs_01_0915]
  - Further, even a small 1mUI error in J_5 or J_6 leads to ~10mUI error in CDJ
- Even-odd jitter has a separate spec. But gets included in CDJ as well
  - The non-EOJ CDJ budget of 21mUI is impractical (~5x less than CAUI-4's 100mUIpp)

Proposed Solution

- Instead of J_5 and J_6, use J_{RMS} and J_5:
  - Defined in healey_3bs_03_0115
  - Use {0, 3} clock pattern or {0, 0, 3, 3} pattern (requires lower equipment b/w)
  - Measure J_{RMS} and J_5 directly
- Exclude even-odd jitter
  - Measure only rising or falling edges if using {0,3} pattern
- Use PRBS31Q on all the other lanes
  - Capture coupling effects from nearby lanes
  - However, the current management infrastructure doesn't support this
- The New specs:

Jitter Type	Amount
JRMS max	0.023 UI
J5 max (pk-pk)	0.128 UI
Even-odd max	0.019 UI

Target for low b/w CRUs

- DSP based receivers prefer a lower CRU b/w spec.
  - Allows higher loop latency for DSP based architectures
  - If the JTOL corner frequency is reduced, the high-pass filter corner frequency for TX jitter measurements should be reduced accordingly
- Should the jitter budgets be revised for the lower b/w CRUs?
- Lab measurements suggest this is may not be needed:
  - Measurement on a large production ASIC with on-board clock source
  - TX jitter increases on lowering the CRU b/w to 2MHz but still within proposed limits
  - Propose to use the current limits pending further review

Conclusions

- Direct measurement of JRMS and J5 is a superior alternative to the existing method.
  - Eliminates the possible extrapolation error
- De-coupling EOJ and DJ makes the TX jitter budget practical.
- Use of lower frequency clock patterns relaxes the test equipment requirements
- Lowering the CRU b/w to 2MHz can be accommodated