118.4 Protocol implementation conformance statement (PICS) proforma for Clause 118, CCMII Extender, CDMII Extender, CCMII Extender Sublayer (CCXS), and CDMII Extender Sublayer (CDXS)[2]

118.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 118, CCMII Extender, CDMII Extender, CCMII Extender Sublayer (CCXS), and CDMII Extender Sublayer (CDXS), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

118.4.2 Identification

118.4.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

118.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bs-201x, Clause 118, CCMII Extender, CDMII Extender, CCMII Extender Sublayer (CCXS), and CDMII Extender Sublayer (CDXS)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bs-201x.)	

Date of Statement	

[2]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

118.4.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
Item	Feature	Subclause	Value/Comment	Status	Support
CCE200	CCMII logical interface	117, 119.1.4.1	Logical interface is supported	O	Yes [ ] No [ ]
CDE400	CDMII logical interface	117, 119.1.4.1	Logical interface is supported	O	Yes [ ] No [ ]
*CCXS	Using the XS for 200GBASE-R	119.1.1		O	Yes [ ] No [ ]
*CDXS	Using the XS for 400GBASE-R	119.1.1		O	Yes [ ] No [ ]
*MD	MDIO	45, 118.3	Registers and interface supported	O	Yes [ ] No [ ]
BEC	Bypass error correction	119.2.5.3	Capability is supported	O	Yes [ ] No [ ]
DC	Delay constraints	119.5	Conforms to delay constraints specified in 119.5	M	Yes [ ]
EEE	EEE capability	119.2.3.3	Capability is supported	O	Yes [ ] No [ ]
JTM	Supports test-pattern mode	118.4.5		M	Yes [ ] No [ ]

118.4.4 PICS proforma tables for CCMII Extender, CDMII Extender, CCMII Extender Sublayer (CCXS), and CDMII Extender Sublayer (CDXS)

118.4.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	64B/66B to 256B/257B transcoder	119.2.4.2	tx_xcoded<256:0> constructed per 119.2.4.2	M	Yes [ ]
TF2	Transmission bit ordering	119.2.4.8	First bit transmitted is bit 0	M	Yes [ ]
TF3	Pad value	119.2.4.4	PRBS9	M	Yes [ ]
TF4	Alignment marker insertion	119.2.4.4		M	Yes [ ]
TF5	Pre-FEC distribution	119.2.4.5	Distribute the data to two FEC codewords	M	Yes [ ]
TF6	Reed-Solomon encoder	119.2.4.6	RS(544,514)	M	Yes [ ]
TF7	Symbol distribution	119.2.4.7	Distribution is based on 10b symbols	M	Yes [ ]

118.4.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	119.2.5.1	Maximum Skew of 180 ns between PCS lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder and de-interleave	119.2.5.2	Order the PCS lanes according to the PCS lane number and de-interleave the FEC codewords	M	Yes [ ]
RF3	Reed-Solomon decoder	119.2.5.3	Corrects any combination of up to t=15 symbol errors in a codeword	M	Yes [ ]
RF4	Reed-Solomon decoder	119.2.5.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF5	Error indication function	119.2.5.3	Corrupts 66-bit block synchronization headers for uncorrected errored codewords (or errored codewords when correction is bypassed)	M	Yes [ ]
RF6	Support for optional bypass indication	119.2.5.3	In the FEC decoder optionally bypass indication can be supported (no marking of frames from uncorrectable codewords)	O	Yes [ ] No [ ]
RF7	256B/257B to 64B/66B transcoder	119.2.5.7	rx_coded_j<65:0>, j=0 to 3 constructed per 119.2.5.7	M	Yes [ ]

118.4.4.3 64B/66B Coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder (and ENCODE function) implements the code as specified	119.2.3 and 119.2.6.2.3		M	Yes [ ] No [ ]
C2	Decoder (and DECODE function) implements the code as specified	119.2.3 and 119.2.6.2.3		M	Yes [ ] No [ ]
C3	Only valid block types are transmitted	119.2.3.2		M	Yes [ ] No [ ]
C4	Invalid block types are treated as an error	119.2.3.2		M	Yes [ ] No [ ]
C5	Only valid control characters are transmitted	119.2.3.3		M	Yes [ ] No [ ]
C6	Invalid control characters are treated as an error	119.2.3.3		M	Yes [ ] No [ ]
C7	Idles do not interrupt data	119.2.3.5		M	Yes [ ] No [ ]
C8	IDLE control code insertion and deletion	119.2.3.5	Insertion or Deletion in groups of 8 /I/s	M	Yes [ ] No [ ]
C9	Sequence ordered set deletion	119.2.3.8	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ] No [ ]

118.4.4.4 Scrambler and Descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	119.2.4.3	Performs as shown in Figure 49–8	M	Yes [ ] No [ ]
S2	Descrambler	119.2.5.6	Performs as shown in Figure 49–10	M	Yes [ ] No [ ]

118.4.4.5 Alignment Markers

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Alignment marker insertion	119.2.4.4	Alignment markers are inserted periodically as described in section 119.2.4.4	M	Yes [ ] No [ ]
AM2	Alignment marker form	119.2.4.4	Alignment markers are formed as described in section 119.2.4.4	M	Yes [ ] No [ ]
AM3	Lane mapping	119.2.6.3	PCS lane number is captured	MD:M	Yes [ ] No [ ]

118.4.5 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Scrambled idle transmit test-pattern generator is implemented	119.2.4.9		M	Yes [ ] No [ ] N/A[ ]

118.4.5.1 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	119.2.4.8	Placement of bits into the PCS lanes as shown in Figure 119–10 or Figure 119–11	M	Yes [ ] No [ ]

118.4.6 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Alternate access to XS Management objects is provided	119.3		O	Yes [ ] No [ ]

118.4.6.1 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Alignment Marker Lock	119.2.6	Implements 8 alignment marker lock processes as depicted in Figure 119–12	CCXS:M	Yes [ ] No [ ]
SM2	Alignment Marker Lock	119.2.6	Implements 16 alignment marker lock processes as depicted in Figure 119–12	CDXS:M	Yes [ ] No [ ]
SM3	The SLIP functions evaluates all possible blocks	119.2.6.2.3		M	Yes [ ] No [ ]
SM4	PCS synchronization state diagram	119.2.6	Meets the requirements of Figure 119–13	M	Yes [ ] No [ ]
SM5	Transmit process	119.2.6	Meets the requirements of Figure 119–14	M	Yes [ ] No [ ]
SM6	Receive process	119.2.6	Meets the requirements of Figure 119–15	M	Yes [ ] No [ ]

118.4.6.2 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports loopback	119.4		M	Yes [ ] No [ ] N/A[ ]
L2	When in loopback, transmits what it receives from the CCMII/CDMII	119.4		M	Yes [ ] No [ ]

118.4.6.3 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS Delay Constraint	119.5	No more than 160 256 BT for sum of transmit and receive path delays for 200GBASE-R.	CCXS: M	Yes [ ] No [ ]
TIM2	PCS Delay Constraint	119.5	No more than 320 000 BT for sum of transmit and receive path delays for 400GBASE-R.	CDXS: M	Yes [ ] No [ ]