CDAUI-8 Chip-to-chip Jitter Budget Proposal

In support of Comment # 42

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Motivation

- Current specification in Table 120D-1

Jitter Type	Amount
CRJ max (RMS)	0.01 UI
CDJ max (pk-pk)	0.04 UI
Even-odd max	0.019 UI

- Measurement method employed is specified in 94.3.12.6
  - For CRJ and CDJ:
    - JP03A test pattern – repeating {0, 3} sequence
    - Extraction using J_5 and J_6

$$\begin{bmatrix} CRJrms \\ CDJ \end{bmatrix} = \begin{bmatrix} 1.0538 & -1.0538 \\ -9.3098 & 10.3098 \end{bmatrix} \begin{bmatrix} J_6 \\ J_5 \end{bmatrix}$$

- Extrapolation from J_5 and J_6 is not reliable
  - Concerns raised in [healey_3bs_01_0915]
  - Further, even a small 1mUI error in J_5 or J_6 leads to ~10mUI error in CDJ

Proposed Solution

- Instead of J_5 and J_6, use J_{RMS} and J_5:
  - Defined in healey_3bs_03_0115
  - Use JP03A test pattern
  - Measure J_{RMS} and J_5 directly
- Use PRBS31Q on all the other lanes
  - Capture coupling effects from nearby lanes
  - However, the current management infrastructure doesn't support this
- The New specs:

Jitter Type	Amount
JRMS max	0.023 UI
J5 max (pk-pk)	0.128 UI
Even-odd max	0.019 UI