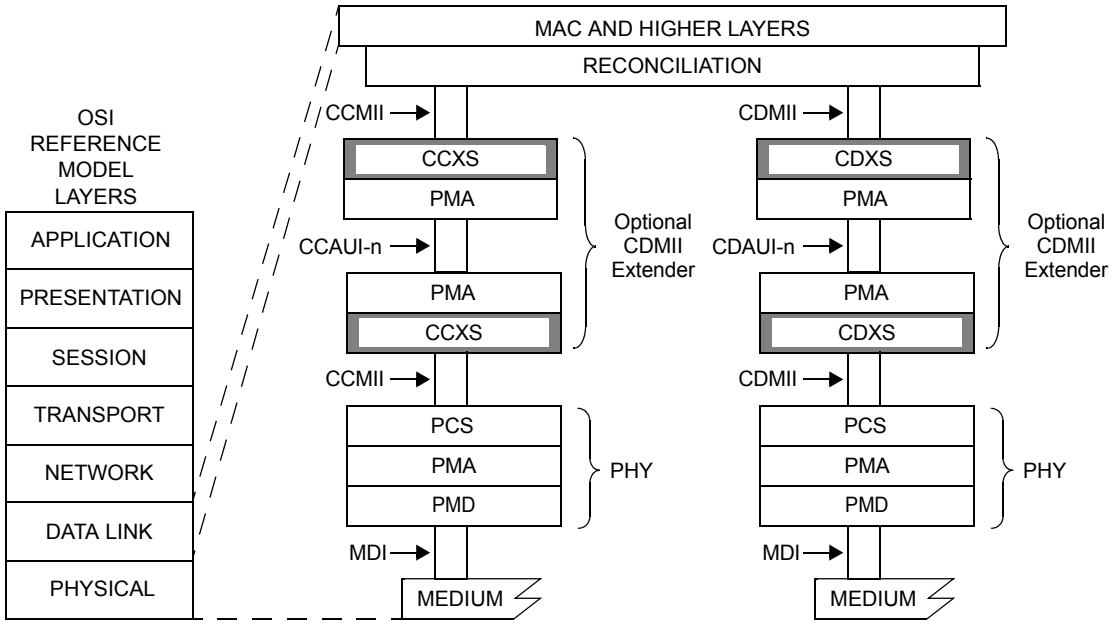
118. CCMII Extender, CDMII Extender, CCMII Extender Sublayer (CCXS), and CDMII Extender Sublayer (CDXS)

118.1 Overview

This clause defines the functional characteristics for the optional CCMII Extender and CCMII Extender Sublayer (CCXS), and also for the optional CDMII Extender and CDMII Extender Sublayer (CDXS). Figure 118–1 shows the relationship of the CCMII/CDMII Extender and CCXS/CDXS sublayer with other sublayers to the ISO Open System Interconnection (OSI) reference model.

The CCMII/CDMII Extender allows the extension of the CCMII/CDMII to the PCS via a physical instantiation. The CCMII/CDMII Extender is composed of a CCXS/CDXS at the RS end, a CCXS/CDXS at the PHY end with a physical instantiation of CCAUI-n/CDAUI-n between two adjacent PMA sublayers.

A CCMII/CDMII Extender with the optional Energy-Efficient Ethernet (EEE) capability (see Clause 78) encodes and decodes Low Power Idle (LPI) signals. The assertion of LPI at the CCMII/CDMII is encoded in the transmitted symbols. Detection of LPI encoding in the received symbols is indicated as LPI at the CCMII/CDMII.



CCAUI-n = 200 Gb/s n-LANE ATTACHMENT UNIT INTERFACE
CCMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
CCXS = CCMII EXTENDER SUBLAYER
CDAUI-n = 400 Gb/s n-LANE ATTACHMENT UNIT INTERFACE
CDMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
CDXS = CDMII EXTENDER SUBLAYER
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 118–1—CCXS and CDXS relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 Ethernet model

118.1.1 Summary of major concepts

The following is a list of the major concepts of the CCMII/CDMII Extender:

a) Simple signal mapping to the CCMII/CDMII

b) The optional CCMII/CDMII Extender can be inserted between the Reconciliation Sublayer and the PHY to transparently extend the reach of the CCMII/CDMII

c) Independent transmit and receive data paths

d) The CDXS/CDXS leverages all functions in the Clause 119 PCS and supports physical instantiations of the CCAUI-n/CDAUI-n

e) Optionally extends LPI signaling to the PHY for EEE

118.1.2 CCXS/CDXS Sublayer

The CCXS is identical in function to the 200GBASE-R PCS in Clause 119 with the addition of the functions defined in 118.2 and the CDXS is identical in function to the 400GBASE-R PCS in Clause 119 with the addition of the functions defined in 118.2.

118.1.3 CCAUI-n/CDAUI-n

A CCMII Extender may use any of the following physical instantiations of the CCAUI-n:

— CCAUI-8 chip-to-chip (Annex 120B)
— CCAUI-8 chip-to-module (Annex 120C)
— CCAUI-4 chip-to-chip (Annex 120D)
— CCAUI-4 chip-to-module (Annex 120E)

A CDMII Extender may use any of the following physical instantiations of the CDAUI-n:

— CDAUI-16 chip-to-chip (Annex 120B)
— CDAUI-16 chip-to-module (Annex 120C)
— CDAUI-8 chip-to-chip (Annex 120D)
— CDAUI-8 chip-to-module (Annex 120E)

118.2 FEC Degrade

In addition to the optional FEC degrade functionality that is described in Clause 119, the DTE CCXS or DTE CDXS optionally performs the extra functions described in 118.2.1. Instead of the optional FEC degrade functionality that is described in Clause 119, the PHY CCXS or PHY CDXS optionally performs the functions described in 118.2.2.

118.2.1 DTE XS FEC Degrade signaling

When FEC_degraded_SER_enable (see 118.3) is asserted, the DTE CCXS or DTE CDXS performs the following additional functions.

rx_local_degraded
: Boolean variable that is asserted true when the receiver detects rx_am_sf<1> asserted true for two consecutive alignment marker periods. It is deasserted when rx_am_sf<1> is deasserted for two consecutive alignment marker periods. If a Clause 45 MDIO is implemented, the status of this variable is reflected in bit 5.801.6 of the DTE XS FEC status register.

The variable tx_am_sf is set as follows:

tx_am_sf<2:0> = {FEC_degraded_SER + rx_local_degraded,0,0}

118.2.2 PHY XS FEC Degrade signaling

When FEC_degraded_SER_enable (see 118.3) is asserted, the PHY CCXS or PHY CDXS performs the following functions instead of setting tx_am_sf<2:0> as in 119.2.4.4.

The behavior of the PHY CCXS or PHY CDXS is depicted in Figure 118–2 and Figure 118–3.

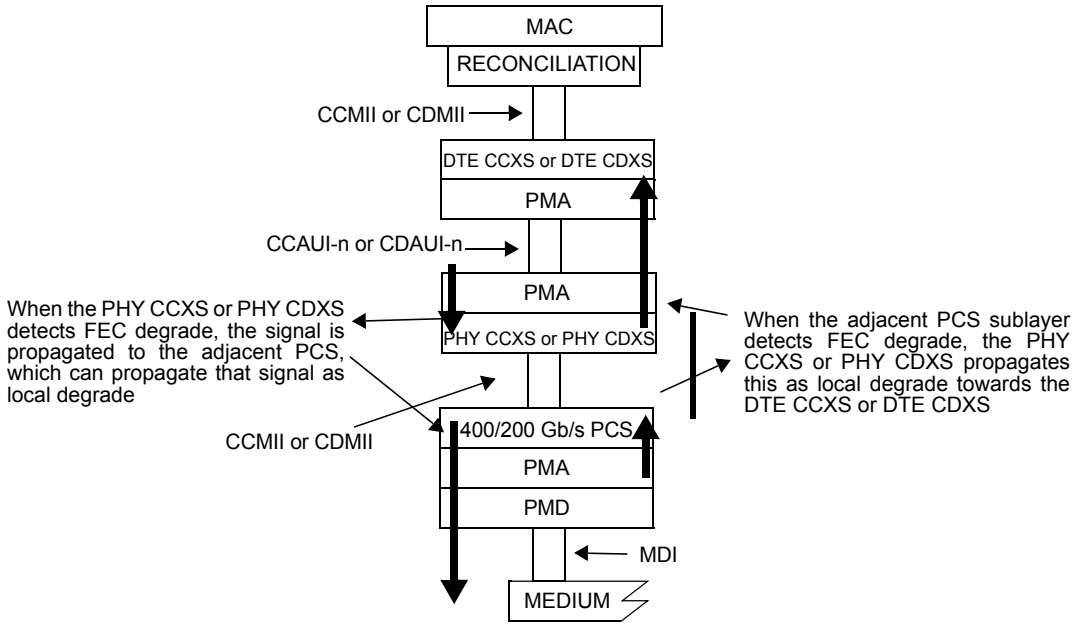


Figure 118–2—PHY XS FEC Degrade detection

FEC_degraded_SER is still declared as described in 119.2.5.3 but it is also used to inform the adjacent PCS sublayer of the FEC degrade state of the PHY XS.

adjacent_pcs_local_degraded
: Boolean variable that is asserted true when the adjacent PCS sublayer indicates is has FEC local degraded active (its equivalent to the FEC_degraded_SER variable is asserted or its equivalent to the rx_local_degraded variable is asserted).

adjacent_pcs_rm_degraded
: Boolean variable that is asserted true when the adjacent PCS sublayer indicates is has FEC remote degraded active (its equivalent to the rx_rm_degraded variable is asserted).

The variable tx_am_sf is set as follows:
tx_am_sf<2:0> = {adjacent_pcs_rm_degraded, adjacent_pcs_local_degraded, 0}

rx_rm_degraded
: Boolean variable that is asserted true when the receiver detects rx_am_sf<2> asserted true for two consecutive alignment marker periods. It is deasserted when rx_am_sf<2> is deasserted for two consecutive alignment marker periods. This variable is used to inform the adjacent PCS sublayer of the FEC

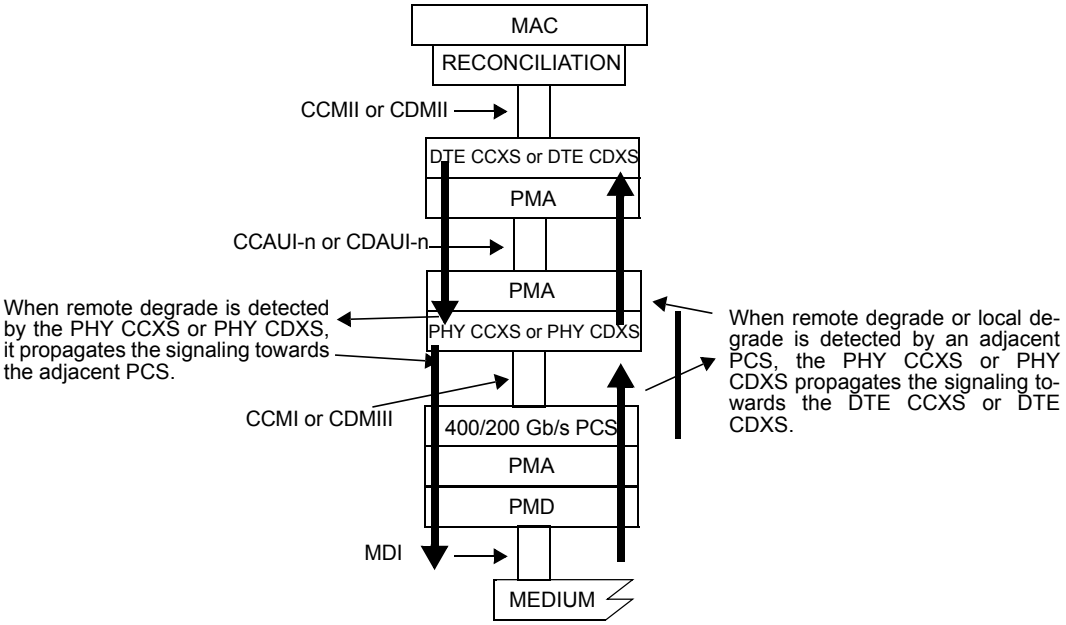


Figure 118–3—PHY XS FEC Degrade propagation

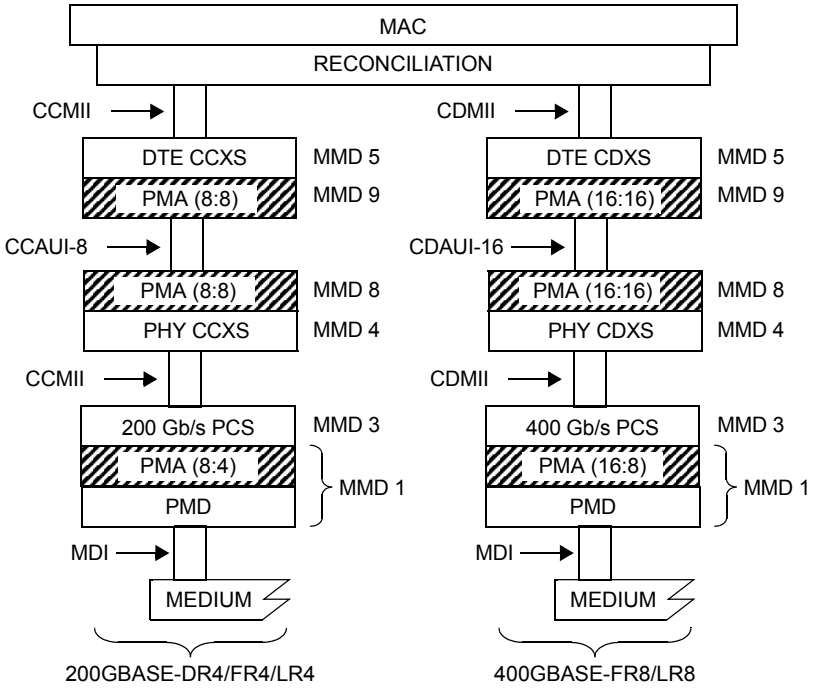
degrade state of the PHY XS. If a Clause 45 MDIO is implemented, the status of this variable is reflected in bit 4.801.5

118.3 CCXS and CDXS partitioning example

A partitioning example and MMD numbering using the CCXS and CDXS is shown in Figure 118–4.

118.4 CCXS and CDXS MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the CCXS or CDXS. If MDIO is implemented, it shall map MDIO PHY XS and DTE XS control bits to Clause 119 control variables as shown in Table 118–1 and Table 118–3, respectively. Similarly, if MDIO is implemented, it shall map MDIO PHY XS and DTE XS MDIO status bits to Clause 119 status variables as shown in Table 118–2 and Table 118–4, respectively.



CCAUI = 200 Gb/s ATTACHMENT UNIT INTERFACE
CCMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE
CCXS = 200 Gb/s EXTENDER SUBLAYER
CDAUI = 400 Gb/s ATTACHMENT UNIT INTERFACE
CDMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE
CDXS = 400 Gb/s EXTENDER SUBLAYER
DTE = DATA TERMINAL EQUIPMENT
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
MMD = MDIO MANAGEABLE DEVICE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT

Figure 118–4—Example 200GBASE-DR4/FR4/LR4 and 400GBASE-FR8/LR8 PMA layering with CCXS and CDXS

Table 118–1—MDIO PHY XS to Clause 119 control variable mapping

MDIO control variable	PCS register name	Register/ bit number	Clause 119 control variable
Reset	PHY XS control 1 register	4.0.15	reset
Loopback	PHY XS control 1 register	4.0.14	Loopback
Transmit test-pattern enable	BASE-R PHY XS test-pattern control register	4.42.3	tx_test_mode
Receive test-pattern enable	BASE-R PHY XS test-pattern control register	4.42.2	rx_test_mode
PHY XS FEC bypass indication enable	PHY XS FEC control register	4.800.1	FEC_bypass_indication_enable
PHY XS FEC degraded SER enable	PHY XS FEC control register	4.800.2	FEC_degraded_SER_enable
PHY XS FEC degraded SER activate threshold	PHY XS FEC degraded SER activate threshold register	4.806, 4.807	FEC_degraded_SER_activate_threshold
PHY XS FEC degraded SER deactivate threshold	PHY XS FEC degraded SER deactivate threshold register	4.808, 4.809	FEC_degraded_SER_deactivate_threshold
PHY XS FEC degraded SER interval	PHY XS FEC degraded SER interval	4.810, 4.811	FEC_degraded_SER_interval

Table 118–2—MDIO PHY XS to Clause 119 status variable mapping

MDIO status variable	PCS register name	Register/ bit number	Clause 119 status variable
BASE-R PHY XS receive link status	BASE-R PHY XS status 1	4.32.12	PCS_status
Lane *x* aligned	Multi-lane BASE-R PHY XS alignment status 3 and 4	4.52.7:0 4.53.7:0	am_lock<*x*>
PHY XS lane alignment status	Multi-lane BASE-R PHY XS alignment status 1	4.50.12	align_status
Lane *x* mapping	PHY XS lane mapping, lane 0 through lane 15	4.400 through 4.415	lane_mapping
PHY XS FEC bypass indication ability	PHY XS FEC status	4.801.1	FEC_bypass_indication_ability
FEC corrected codewords	PHY XS FEC corrected codewords counter	4.802, 4.803	FEC_corrected_cw_counter
FEC uncorrected codewords	PHY XS FEC uncorrected codewords counter	4.804, 4.805	FEC_uncorrected_cw_counter
PHY XS FEC symbol errors, lane 0 to lane 15	PHY XS FEC symbol error counter, lane 0 to lane 15	4.600 to 4.631	FEC_symbol_error_counter_*i*

Table 118–2—MDIO PHY XS to Clause 119 status variable mapping *(continued)*

MDIO status variable	PCS register name	Register/ bit number	Clause 119 status variable
Tx LPI indication	PHY XS status 1	4.1.9	Tx LPI indication
Tx LPI received	PHY XS status 1	4.1.11	Tx LPI received
Rx LPI indication	PHY XS status 1	4.1.8	Rx LPI indication
Rx LPI received	PHY XS status 1	4.1.10	Rx LPI received
EEE wake error counter	EEE wake error counter	4.22	Wake_error_counter
PHY XS FEC degraded SER ability	PHY XS FEC status register	4.801.3	FEC_degraded_SER_ability
PHY XS FEC degraded SER	PHY XS FEC status register	4.801.4	FEC_degraded_SER
Remote degraded SER received	PHY XS FEC status register	4.801.5	rx_rm_degraded

Table 118–3—MDIO DTE XS to Clause 119 control variable mapping

MDIO control variable	PCS register name	Register/ bit number	Clause 119 control variable
Reset	DTE XS control 1 register	5.0.15	reset
Loopback	DTE XS control 1 register	5.0.14	Loopback
Transmit test-pattern enable	BASE-R DTE XS test-pattern control register	5.42.3	tx_test_mode
Receive test-pattern enable	BASE-R DTE XS test-pattern control register	5.42.2	rx_test_mode
DTE XS FEC bypass indication enable	DTE XS FEC control register	5.800.1	FEC_bypass_indication_enable
DTE XS FEC degraded SER enable	DTE XS FEC control register	5.800.2	FEC_degraded_SER_enable
DTE XS FEC degraded SER activate threshold	DTE XS FEC degraded SER activate threshold register	5.806, 5.807	FEC_degraded_SER_activate_threshold
DTE XS FEC degraded SER deactivate threshold	DTE XS FEC degraded SER deactivate threshold register	5.808, 5.809	FEC_degraded_SER_deactivate_threshold
DTE XS FEC degraded SER interval	DTE XS FEC degraded SER interval	5.810, 5.811	FEC_degraded_SER_interval

Table 118–4—MDIO DTE XS to Clause 119 status variable mapping

MDIO status variable	PCS register name	Register/ bit number	Clause 119 status variable
BASE-R DTE XS receive link status	BASE-R DTE XS status 1	5.32.12	PCS_status
Lane *x* aligned	Multi-lane BASE-R DTE XS alignment status 3 and 4	5.52.7:0 5.53.7:0	am_lock<*x*>
DTE XS lane alignment status	Multi-lane BASE-R DTE XS alignment status 1	5.50.12	align_status
Lane *x* mapping	DTE XS lane mapping, lane 0 through lane 15	5.400 through 5.415	lane_mapping
DTE XS FEC bypass indication ability	DTE XS FEC status	5.801.1	FEC_bypass_indication_ability
FEC corrected codewords	DTE XS FEC corrected codewords counter	5.802, 5.803	FEC_corrected_cw_counter
FEC uncorrected codewords	DTE XS FEC uncorrected codewords counter	5.804, 5.805	FEC_uncorrected_cw_counter
DTE XS FEC symbol errors, lane 0 to lane 15	DTE XS FEC symbol error counter, lane 0 to lane 15	5.600 to 5.631	FEC_symbol_error_counter_*i*
Tx LPI indication	DTE XS status 1	5.1.9	Tx LPI indication
Tx LPI received	DTE XS status 1	5.1.11	Tx LPI received
Rx LPI indication	DTE XS status 1	5.1.8	Rx LPI indication
Rx LPI received	DTE XS status 1	5.1.10	Rx LPI received
EEE wake error counter	EEE wake error counter	5.22	Wake_error_counter
DTE XS FEC degraded SER ability	DTE XS FEC status register	5.801.3	FEC_degraded_SER_ability
DTE XS FEC degraded SER	DTE XS FEC status register	5.801.4	FEC_degraded_SER
Remote degraded received	DTE XS FEC status register	5.801.5	rx_rm_degraded
Local degraded received	DTE XS FEC status register	5.801.6	rx_local_degraded

118.5 Protocol implementation conformance statement (PICS) proforma for Clause 118, CCMII Extender, CDMII Extender, CCMII Extender Sublayer (CCXS), and CDMII Extender Sublayer (CDXS)[2]

118.5.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 118, CCMII Extender, CDMII Extender, CCMII Extender Sublayer (CCXS), and CDMII Extender Sublayer (CDXS), shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

118.5.2 Identification

118.5.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

118.5.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3bs-201x, Clause 118, CCMII Extender, CDMII Extender, CCMII Extender Sublayer (CCXS), and CDMII Extender Sublayer (CDXS)
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bs-201x.)	

Date of Statement	

[2]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

118.5.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
Item	**Feature**	**Subclause**	**Value/Comment**	**Status**	**Support**
CCE200	CCMII logical interface	117, 119.1.4.1	Logical interface is supported	O	Yes [ ] No [ ]
CDE400	CDMII logical interface	117, 119.1.4.1	Logical interface is supported	O	Yes [ ] No [ ]
*CCXS	Using the XS for 200GBASE-R	119.1.1		O	Yes [ ] No [ ]
*CDXS	Using the XS for 400GBASE-R	119.1.1		O	Yes [ ] No [ ]
*MD	MDIO	45, 118.4	Registers and interface supported	O	Yes [ ] No [ ]
BEC	Bypass error correction	119.2.5.3	Capability is supported	O	Yes [ ] No [ ]
DC	Delay constraints	119.5	Conforms to delay constraints specified in 119.5	M	Yes [ ]
EEE	EEE capability	119.2.3.3	Capability is supported	O	Yes [ ] No [ ]
JTM	Supports test-pattern mode	118.5.5		M	Yes [ ] No [ ]

118.5.4 PICS proforma tables for CCMII Extender, CDMII Extender, CCMII Extender Sublayer (CCXS), and CDMII Extender Sublayer (CDXS)

118.5.4.1 Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
TF1	64B/66B to 256B/257B transcoder	119.2.4.2	tx_xcoded<256:0> constructed per 119.2.4.2	M	Yes [ ]
TF2	Transmission bit ordering	119.2.4.8	First bit transmitted is bit 0	M	Yes [ ]
TF3	Pad value	119.2.4.4	PRBS9	M	Yes [ ]
TF4	Alignment marker insertion	119.2.4.4		M	Yes [ ]
TF5	Pre-FEC distribution	119.2.4.5	Distribute the data to two FEC codewords	M	Yes [ ]
TF6	Reed-Solomon encoder	119.2.4.6	RS(544,514)	M	Yes [ ]
TF7	Symbol distribution	119.2.4.7	Distribution is based on 10b symbols	M	Yes [ ]

118.5.4.2 Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
RF1	Skew tolerance	119.2.5.1	Maximum Skew of 180 ns between PCS lanes and a maximum Skew Variation of 4 ns	M	Yes [ ]
RF2	Lane reorder and de-interleave	119.2.5.2	Order the PCS lanes according to the PCS lane number and de-interleave the FEC codewords	M	Yes [ ]
RF3	Reed-Solomon decoder	119.2.5.3	Corrects any combination of up to t=15 symbol errors in a codeword	M	Yes [ ]
RF4	Reed-Solomon decoder	119.2.5.3	Capable of indicating when a codeword was not corrected.	M	Yes [ ]
RF5	Error indication function	119.2.5.3	Corrupts 66-bit block synchronization headers for uncorrected errored codewords (or errored codewords when correction is bypassed)	M	Yes [ ]
RF6	Support for optional bypass indication	119.2.5.3	In the FEC decoder optionally bypass indication can be supported (no marking of frames from uncorrectable codewords)	O	Yes [ ] No [ ]
RF7	256B/257B to 64B/66B transcoder	119.2.5.7	rx_coded_j<65:0>, j=0 to 3 constructed per 119.2.5.7	M	Yes [ ]
RF8	Support for optional FEC Degraded detection	119.2.5.3 118.2	In the FEC decoder can optionally detect FEC degraded at a programmable threshold	O	Yes [ ] No [ ]

118.5.4.3 64B/66B Coding rules

Item	Feature	Subclause	Value/Comment	Status	Support
C1	Encoder (and ENCODE function) implements the code as specified	119.2.3 and 119.2.6.2.3		M	Yes [ ] No [ ]
C2	Decoder (and DECODE function) implements the code as specified	119.2.3 and 119.2.6.2.3		M	Yes [ ] No [ ]
C3	Only valid block types are transmitted	119.2.3.2		M	Yes [ ] No [ ]
C4	Invalid block types are treated as an error	119.2.3.2		M	Yes [ ] No [ ]
C5	Only valid control characters are transmitted	119.2.3.3		M	Yes [ ] No [ ]
C6	Invalid control characters are treated as an error	119.2.3.3		M	Yes [ ] No [ ]
C7	Idles do not interrupt data	119.2.3.5		M	Yes [ ] No [ ]
C8	IDLE control code insertion and deletion	119.2.3.5	Insertion or Deletion in groups of 8 /I/s	M	Yes [ ] No [ ]
C9	Sequence ordered set deletion	119.2.3.8	Only one whole ordered set of two consecutive sequence ordered sets may be deleted	M	Yes [ ] No [ ]

118.5.4.4 Scrambler and Descrambler

Item	Feature	Subclause	Value/Comment	Status	Support
S1	Scrambler	119.2.4.3	Performs as shown in Figure 49–8	M	Yes [ ] No [ ]
S2	Descrambler	119.2.5.6	Performs as shown in Figure 49–10	M	Yes [ ] No [ ]

118.5.4.5 Alignment Markers

Item	Feature	Subclause	Value/Comment	Status	Support
AM1	Alignment marker insertion	119.2.4.4	Alignment markers are inserted periodically as described in section 119.2.4.4	M	Yes [ ] No [ ]
AM2	Alignment marker form	119.2.4.4	Alignment markers are formed as described in section 119.2.4.4	M	Yes [ ] No [ ]
AM3	Lane mapping	119.2.6.3	PCS lane number is captured	MD:M	Yes [ ] No [ ]

118.5.5 Test-pattern modes

Item	Feature	Subclause	Value/Comment	Status	Support
JT1	Scrambled idle transmit test-pattern generator is implemented	119.2.4.9		M	Yes [ ] No [ ] N/A[ ]

118.5.5.1 Bit order

Item	Feature	Subclause	Value/Comment	Status	Support
B1	Transmit bit order	119.2.4.8	Placement of bits into the PCS lanes as shown in Figure 119–10 or Figure 119–11	M	Yes [ ] No [ ]

118.5.6 Management

Item	Feature	Subclause	Value/Comment	Status	Support
M1	Alternate access to XS Management objects is provided	119.3		O	Yes [ ] No [ ]

118.5.6.1 State diagrams

Item	Feature	Subclause	Value/Comment	Status	Support
SM1	Alignment Marker Lock	119.2.6	Implements 8 alignment marker lock processes as depicted in Figure 119–12	CCXS:M	Yes [ ] No [ ]
SM2	Alignment Marker Lock	119.2.6	Implements 16 alignment marker lock processes as depicted in Figure 119–12	CDXS:M	Yes [ ] No [ ]
SM3	The SLIP functions evaluates all possible blocks	119.2.6.2.3		M	Yes [ ] No [ ]
SM4	PCS synchronization state diagram	119.2.6	Meets the requirements of Figure 119–13	M	Yes [ ] No [ ]
SM5	Transmit process	119.2.6	Meets the requirements of Figure 119–14	M	Yes [ ] No [ ]
SM6	Receive process	119.2.6	Meets the requirements of Figure 119–15	M	Yes [ ] No [ ]

118.5.6.2 Loopback

Item	Feature	Subclause	Value/Comment	Status	Support
L1	Supports loopback	119.4		M	Yes [ ] No [ ] N/A[ ]
L2	When in loopback, transmits what it receives from the CCMII/CDMII	119.4		M	Yes [ ] No [ ]

118.5.6.3 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	PCS Delay Constraint	119.5	No more than 160 256 BT for sum of transmit and receive path delays for 200GBASE-R.	CCXS: M	Yes [ ] No [ ]
TIM2	PCS Delay Constraint	119.5	No more than 320 000 BT for sum of transmit and receive path delays for 400GBASE-R.	CDXS: M	Yes [ ] No [ ]