

# Comments #13 and #14, Figures 119-5 and 119-6

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# Introduction

Comments #13 and #14 against P802.3bs D2.0 propose to replace Figures 119-5 and 119-6 with pairs of figures as shown in gorshe\_3bs\_01\_0916.pdf in [http://www.ieee802.org/3/bs/comments/P802d3bs\\_D2p0\\_attachments.zip](http://www.ieee802.org/3/bs/comments/P802d3bs_D2p0_attachments.zip)

This contribution makes an alternative proposal to modify the existing figures as per the following pages.

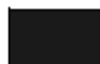
Arrows to show the transmission order have not been added as the actual transmission order depends on any skew between PCS lanes.

# Figure 119-5

PCS lane, $i$	10-bit symbol index, $k$												
	0	1	2	3	4	5	6	7	8	9	10	11	12
0	A	B	A	B	A	B	A	B	A	B	A	B	A
1	B	A	B	A	B	A	B	A	B	A	B	A	B
2	A	B	A	B	A	B	A	B	A	B	A	B	A
3	B	A	B	A	B	A	B	A	B	A	B	A	B
4	A	B	A	B	A	B	A	B	A	B	A	B	A
5	B	A	B	A	B	A	B	A	B	A	B	A	B
6	A	B	A	B	A	B	A	B	A	B	A	B	A
7	B	A	B	A	B	A	B	A	B	A	B	A	B



= 65-bit pad



= 3-bit status field



= Resumption of 257-bit blocks

Figure 119-5—200GBASE-R alignment marker mapping to PCS lanes

# Figure 119-6

PCS lane, $i$	10-bit symbol index, $k$													
	0	1	2	3	4	5	6	7	8	9	10	11		12
0	A	B	A	B	A	B	A	B	A	B	A	B	A	<div style="background-color: #cccccc; width: 100%; height: 100%;"></div>
1	B	A	B	A	B	A	B	A	B	A	B	A	B	
2	A	B	A	B	A	B	A	B	A	B	A	B	A	
3	B	A	B	A	B	A	B	A	B	A	B	A	B	
4	A	B	A	B	A	B	A	B	A	B	A	B	A	
5	B	A	B	A	B	A	B	A	B	A	B	A	B	
6	A	B	A	B	A	B	A	B	A	B	A	B	A	
7	B	A	B	A	B	A	B	A	B	A	B	A	B	
8	A	B	A	B	A	B	A	B	A	B	A	B	A	
9	B	A	B	A	B	A	B	A	B	A	B	A	B	
10	A	B	A	B	A	B	A	B	A	B	A	B	A	
11	B	A	B	A	B	A	B	A	B	A	B	A	B	
12	A	B	A	B	A	B	A	B	A	B	A	B	A	
13	B	A	B	A	B	A	B	A	B	A	B	A	B	
14	A	B	A	B	A	B	A	B	A	B	A	B	A	
15	B	A	B	A	B	A	B	A	B	A	B	A	B	

= 133-bit pad    
  = 3-bit status field    
  = Resumption of 257-bit blocks

**Figure 119-6—400GBASE-R alignment marker mapping to PCS lanes**

Thanks!