Supporting Materials for comment #99

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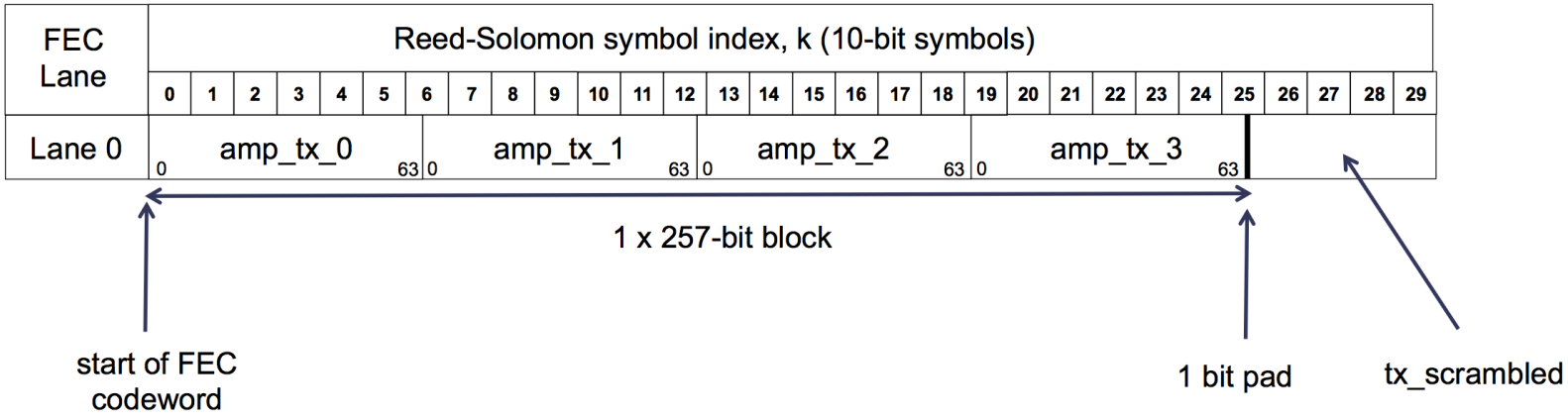
Comment #99

Shift tx_am_sf to be the first nibble of the UP0 for lane 0. Make the 2nd nibble of UP0 for lane 0 be it's inverse. Then 802.3cd can insert it in the single lane implementations in the same "spot".

50GE Baseline (nicholl_3cd_01a_0516.pdf)

50GbE - Alignment marker mapping to FEC lane



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Only a 1bit pad. Where are 3bit of degrade indication going to go?

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Potential solution

- Replace UP0 of all AM0 lanes with 4b degrade signal field (and it's inverse)
  - Provides a common location for all PHYs to look for degrade signaling. Since all PHYs have at least 1 PCS lane, they all would look at bits 37:33 of PCS lane 0 for degrade info.
  - 200G has 4 – 257b AM blocks with a 68b pad
  - 400G has 8 – 257b AM blocks with 136b pad
  - 50G will have 1 – 257b AM block
- Would also provide a location that 25GE could be enhanced to place the information at.
- Would only work for PHYs that don't provide BIP, but the current solution also requires the lack of BIP to provide a Pad space at the end of the AM TC blocks.
- Would limit signally to a 4b field, while current location would allow for expansion beyond 4b.

If we do it

- Following set of slides provide changes needed to move it from end of the AM block into UP0.

119.2.4.4 Paragraph 1

For the 200GBASE-R PCS, an alignment marker group is composed of the alignment markers for all 8 PCS lanes plus an additional 68-bit pad ~~and a 3-bit status field~~ to yield the equivalent of four 257-bit blocks. For the 400GBASE-R PCS, an alignment marker group is composed of the alignment markers for all 16 PCS lanes plus an additional 136-bit pad ~~and a 3-bit status field~~ to yield the equivalent of eight 257-bit blocks.

119.2.4.4

The format of each PCS lane's alignment marker is shown in Figure 119–4. There is a portion that is common across all alignment markers (designated as CM0 to CM5), a unique portion per PCS lane (designated as UM0 to UM5), and finally a unique pad per PCS lane (designated as UP0 to UP2). The 8 bit UP0 for PCS lane 0 transmits the tx_am_sf<3:0> field followed by it's inverse instead of a fixed pad field. Common synchronization logic independent of the received PCS lane number can be used with the common portion of the alignment marker.

119.2.4.4

The transmit alignment marker status field allows the local PCS to communicate the status of the optional FEC degraded feature to the remote PCS. It is set as follows:

~~tx_am_sf<2:0> = {FEC_degraded_SER,0,0}~~

tx_am_sf<3:0> = {0,FEC_degraded_SER,0,0}

119.2.4.4.1

For the 200GBASE-R PCS, the alignment marker mapping function creates a set of 8 alignment markers, and in combination with an additional 68-bit PRBS9 pad ~~and a 3-bit status field~~, the PCS generates an alignment marker group. Let am_*x*<119:0> be the alignment marker for PCS lane *x*, *x*=0 to 7, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_mapped<959:0> in a manner that yields the same result as the following process.

For *x*=0 to 7, am_*x*<119:0> is constructed as follows:

If (x == 0)

am_*x*<119:0> is set to CM0, CM1, CM2, tx_sf_am, ~tx_sf_am, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4 and UM5, as shown in Figure 119–4 (bits 119:0) using the values in Table 119–1 for PCS lane number *0*.

else

am_*x*<119:0> is set to CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4 and UM5, as shown in Figure 119–4 (bits 119:0) using the values in Table 119–1 for PCS lane number *x*.

119.2.4.4.1

As an example, the variable am_1 is sent as (left most bit sent first, showing the first 32 bits transmitted of am_0):

01011001 01010010 01100100 10110011

119.2.4.4.1

The additional 68-bit pad is appended to variable am_mapped as follows:

am_mapped<1027:960> = PRBS9<67:0>

In this expression, PRBS9<0> is the first PRBS9 bit output of the 68-bit pad.

~~The 3-bit transmit alignment marker status field is then appended to the variable am_mapped as follows: am_mapped<1027:1025> = tx_am_sf<2:0>~~

119.2.4.4.2

For the 400GBASE-R PCS, the alignment marker mapping function creates a set of 16 alignment markers, and in combination with an additional 136-bit PRBS9 pad ~~and a 3-bit status field~~, the PCS generates an alignment marker group.

Let am_*x*<119:0> be the alignment marker for PCS lane *x*, *x*=0 to 15, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_mapped<1919:0> in a manner that yields the same result as the following process.

For *x*=0 to *15*,

If (x==0)

am_*x*<119:0> is constructed as follows: am_*x*<119:0> is set to CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4 and UM5, as shown in Figure 119–4 (bits 119:0) using the values in Table 119–2 for PCS lane number *0*.

else

am_*x*<119:0> is constructed as follows: am_*x*<119:0> is set to CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4 and UM5, as shown in Figure 119–4 (bits 119:0) using the values in Table 119–2 for PCS lane number *x*.

119.2.4.4.2

For the 400GBASE-R PCS, the alignment marker mapping function creates a set of 16 alignment markers, and in combination with an additional 136-bit PRBS9 pad ~~and a 3-bit status field~~, the PCS generates an alignment marker group.

Let am_*x*<119:0> be the alignment marker for PCS lane *x*, *x*=0 to 15, where bit 0 is the first bit transmitted. The alignment markers shall be mapped to am_mapped<1919:0> in a manner that yields the same result as the following process.

For *x*=0 to *15*,

If (x==0)

am_*x*<119:0> is constructed as follows: am_*x*<119:0> is set to CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4 and UM5, as shown in Figure 119–4 (bits 119:0) using the values in Table 119–2 for PCS lane number *0*.

else

am_*x*<119:0> is constructed as follows: am_*x*<119:0> is set to CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4 and UM5, as shown in Figure 119–4 (bits 119:0) using the values in Table 119–2 for PCS lane number *x*.

119.2.4.4.2

As an example, the variable am_1 is sent as (left most bit sent first, showing the first 32 bits transmitted of am_0):

01011001 01010010 01100100 00100000

119.2.4.4.2

The additional 136-bit pad is appended to variable am_mapped as follows:

am_mapped<2055:1920> = PRBS9<135:0>

In this expression, PRBS9<0> is the first PRBS9 bit output of the 136-bit pad.

~~The 3-bit transmit alignment marker status field is then appended to the variable am_mapped as follows: am_mapped<2055:2053> = tx_am_sf<2:0>~~

119.2.5.5 Alignment marker removal

For the 200GBASE-R PCS….

rx_am_sf<3:0> = am_rx<37:33>

For the 400GBASE-R PCS….

rx_am_sf<3:0> = am_rx<37:33>

118.2.1

- tx_am_sf<3:0> = {0,FEC_degraded_SER + rx_local_degraded,0,0}

118.2.2

- tx_am_sf<3:0> = {0, adjacent_pcs_rm_degraded, adjacent_pcs_local_degraded, 0}

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