Proposed Reference Equalizer Change in Clause 122.8.5.4 and Test Pattern Change in Table 122-15

Xianxu Peng, Shaoyun Yi, and Winston Way
NeoPhotonics

NeoPhotonics

Supporters

- Vasudevan Parthasarathy, Broadcom
- Rajiv Pancholy, Broadcomm
- Matt Traverso, Cisco
- Marco Mazzini, Cisco
- Frank Chang, InPhi
- Hai-Feng Liu, Intel
- Kohichi Tamura, Oclaro

Introduction

- In testing multiple alpha samples of 400GBase-LR8 transceivers, we found that while a transceiver can pass a 10km link with a sufficient margin, it may not pass the current TDECQ spec in Table 122-10 (Claus 122.7.1) if the reference equalizer follows Claus 122.8.5.4. This causes unnecessary yield loss of EML-based TOSA.

Table 122–10—400GBASE-FR8 and 400GBASE-LR8 transmit characteristics

Description	400GBASE-FR8	400GBASE-LR8	Unit
Signaling rate, each lane (range)	26.5625 ± 100 ppm		GBd
Modulation format	PAM4		—
Lane wavelengths (range)	1272.55 to 1274.54 1276.89 to 1278.89 1281.25 to 1283.27 1285.65 to 1287.68 1294.53 to 1296.59 1299.02 to 1301.09 1303.54 to 1305.63 1308.09 to 1310.19		nm
Side-mode suppression ratio (SMSR), (min)	30		dB
Total average launch power (max)	13.2		dBm
Average launch power, each lane[a] (max)	5.3		dBm
Average launch power, each lane[b] (min)	−5	−2.5	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	5.5	5.7	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min)[c]	0	0.7	dBm
Difference in launch power between any two lanes (OMA_{outer}) (max)	4		dB
Launch power in OMA_{outer} minus TDECQ, each lane (min)	−1	−0.5	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	2.2	2.4	dB
Average launch power of OFF transmitter, each lane (max)	−30		dBm
Extinction ratio (min)	4.5		dB
$RIN_{16.5}OMA$ (max)	−136	—	dB/Hz
$RIN_{17.1}OMA$ (max)	—	−136	dB/Hz
Optical return loss tolerance (max)	16.5	15.1	dB
Transmitter reflectance[d] (max)	−26		dB

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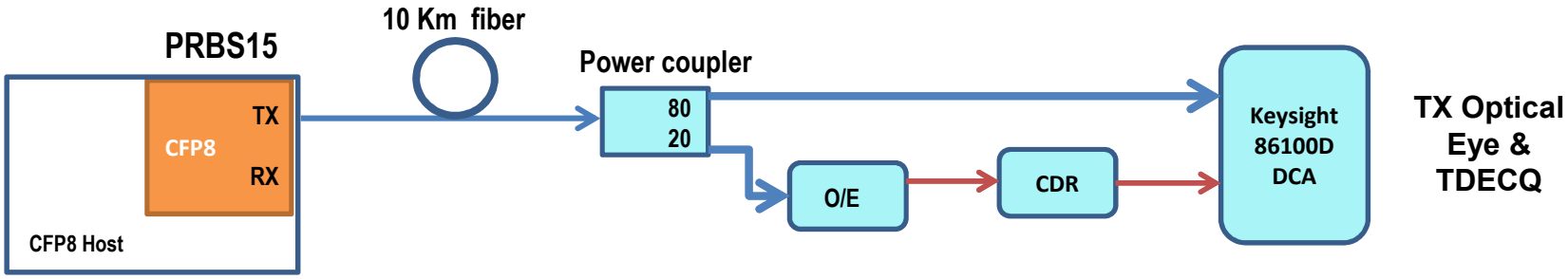
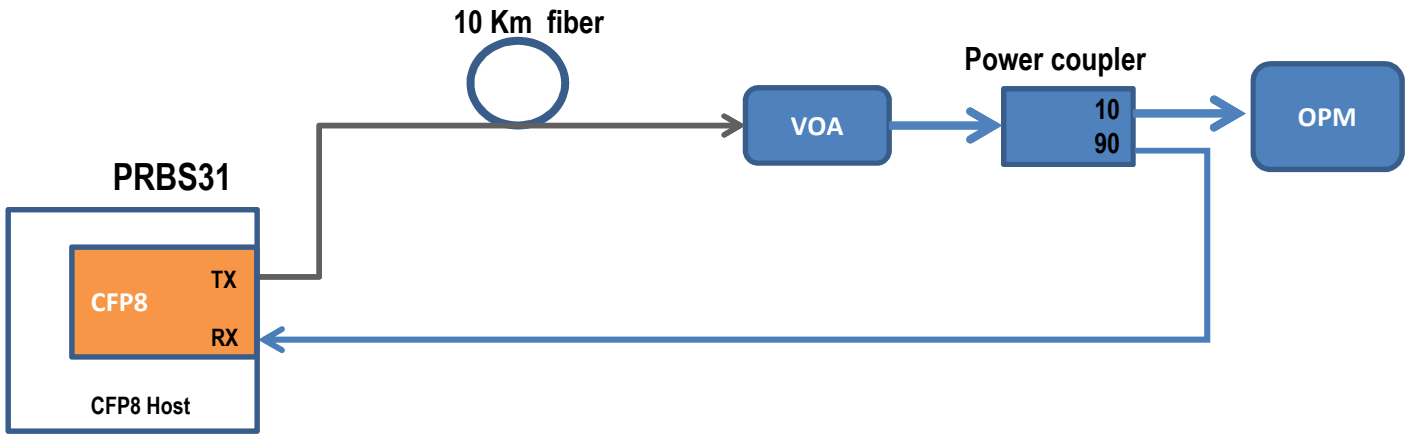
Measurement Setup

- Setup for TDECQ after 10km SMF



- Setup for BER after 10km SMF



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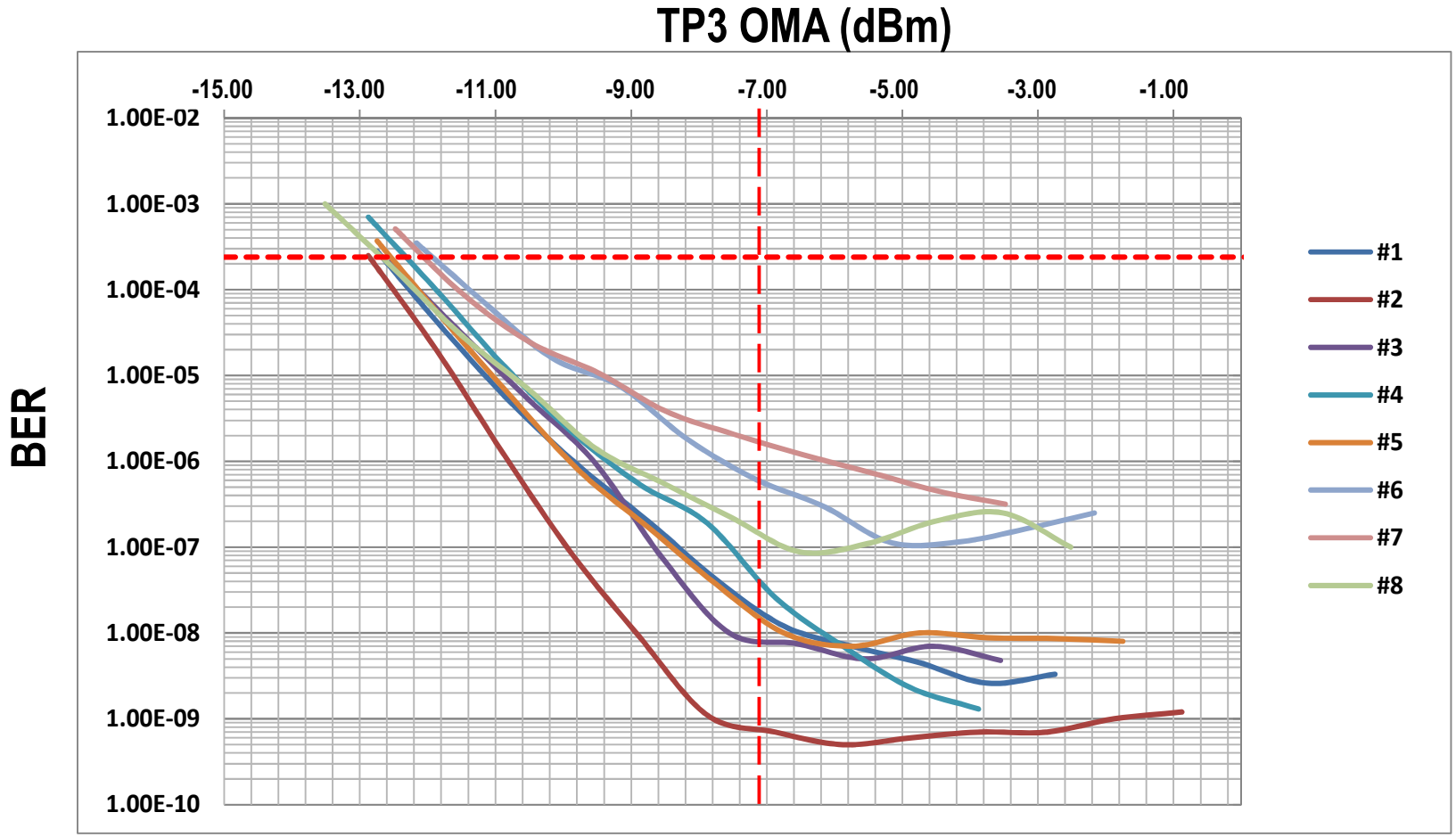
BER versus OMA

- Test results of 8 individual lanes – All pass with sufficient BER and OMA margin



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Corresponding TDECQ using PRBS15

- **There is a reasonable correlation between TDECQ and BER floor (SNR)**
- **TDECQ can meet the 2.4dB spec with 7 and 9 T-spaced taps**
  - All 26.5G PAM4 DSP vendors have implemented >9 T-spaced taps
- **SSPRQ pattern is not available from any existing 8x50G PAM4 chip**
- **Keysight scope does not have sufficient memory to store PRBS31**

Use PRBS15 Or PRBS13Q

BEST LANE

Taps	TOSA#1		TOSA#2		#3		#4		#5	
	T-Space	T/2-Space	T-Space	T/2-Space	T-Space	T/2-Space	T-Space	T/2-Space	T-Space	T/2-Space
5	1.54	3.37	1.64	1.94	2.1	2.59	1.73	2.41	1.61	3.54
7	1.52	1.38	1.55	1.7	2.22	2.23	1.46	1.29	1.53	1.47
9	1.54	1.44	1.32	1.68	2.2	2.19	1.39	1.26	1.46	1.39

Taps	#6		#7		#8	
	T-Space	T/2-Space	T-Space	T/2-Space	T-Space	T/2-Space
5	2.59	3.35	2.69	2.93	2.06	2.53
7	2.29	2.54	2.25	2.43	1.5	1.81
9	1.82	2.51	2.24	2.41	1.58	1.73

2 WORST LANES

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Summary

- **We propose to change Claus 122.8.5.4 from "The reference equalizer for 200GBASE-FR4, 400GBASE-FR8, and 400GBASE-LR8 is a 5 tap, T/2-spaced FFE…" to "The reference equalizer for 200GBASE-FR4, 400GBASE-FR8, and 400GBASE-LR8 is a 7 tap, T-spaced FFE".**
- **Although there is a reasonable correlation between BER floor (SNR) and TDECQ results, the measured TDECQ penalty is unrealistically high. For example, for lane#2 which has a superior BER vs OMA performance, it still incurred 1.32dB TDECQ penalty even the T-spaced tap number is 9. This implies that TDECQ over-estimates link budget penalty.**
- **We propose to change the test pattern of TDECQ in Table 122-15 from SSPRQ to PRBS15 or PRBS13Q.**
  - These pattern generators exist in today's 26.5G PAM4 chips
  - SSPRQ gives even higher TDECQ, which could force the need of more than 7 T-spaced taps.