TX DIFFERENTIAL PRECODER SIMULATION RESULTS & PROPOSAL FOR CDAUI-8 C2C

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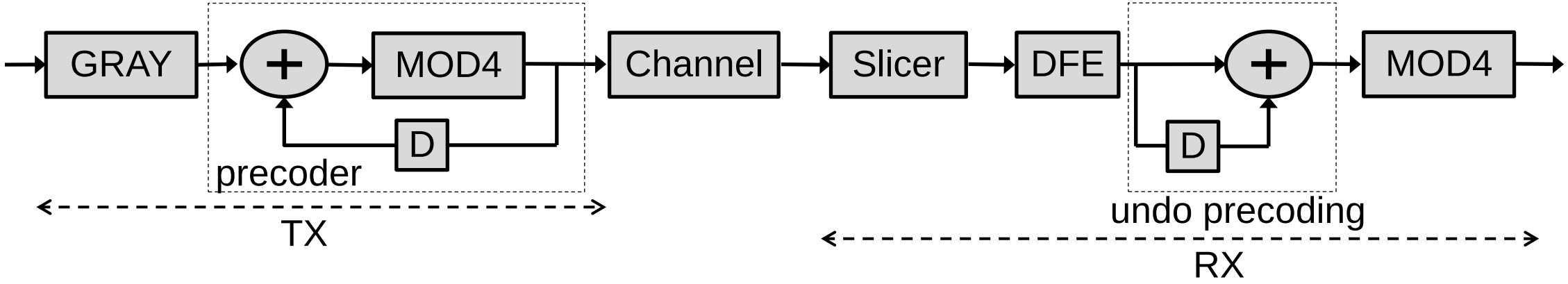
INTRODUCTION



- **Burst Error in the DFE:**
  - Probability of k consecutive errors is a function of the first tap value:
    - Tap value of 1: 0.75^k, Tap value of 0.7: 0.72^k, Tap value of 0.6: 0.62^k
- **Differential Precoder reduces 1-tap DFE burst error runs into 2 errors per event**
  - One error at the entry and one error at the exit
  - Very useful in breaking up long bursts spanning multiple FEC code words.

BER TARGET IMPROVEMENT: NON-INTERLEAVED CASE

For electrical sub-links in Multi-Part links with a penalty of ~0.1dB in the optical sub-link

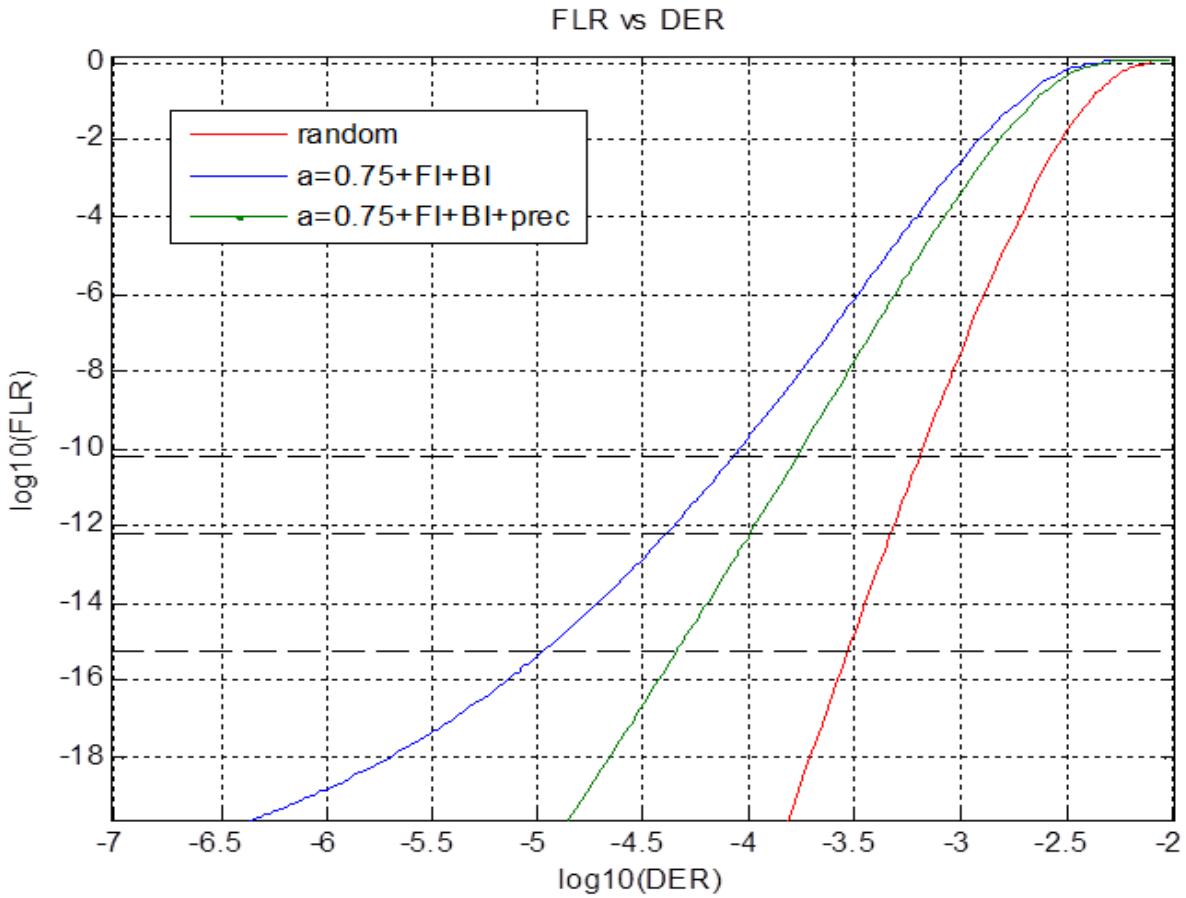
	FLR = 6.2e-11	
	DER0	**BER**
Random (No DFE)	1.60E-04	8.02E-05
a=0.5	5.19E-05	5.19E-05
a=0.75	3.67E-07	7.34E-07
a=0.75 precoded	2.66E-05	2.66E-05

DER0 is the Detector Error Ratio as defined in COM

- Almost 2 orders of magnitude improvement in DER0/BER for DFE tap value ~ 0.7 to 1.0

BER TARGET IMPROVEMENT: INTERLEAVED CASE

Option 8 from anslow_3bs_03_0915: Symbol interleave from 2 FEC code words and bit-muxing in the PMA



- Precoder allows 2X relaxation in DER at FLR = 1e-11
- 4X relaxation possible at FLR = 1e-15

PRECODER IMPLEMENTATION

- **Purely digital implementation**
- **Area estimate and gate-count for different levels of parallelization**

	10T (10 symbols/10T cycle)	16T	20T	32T
design area (um^2)	45	51	60	75
Gate count (NAND2X1 equivalent)	248	281	330	413

- **Timing closure wasn't an issue as well on a commercially available advanced CMOS process node.**

PROPOSAL

- **Requesting the optional-use precoder only for the CDAUI8 chip-to-chip TX PMA**
  - NOT for chip-to-module
  - NOT for the optical portion of the link
- **Re-use the language in 100G-BaseKP4 (94.2.2.6)**
  - The first line will be “The PMA transmit process shall allow for precoding of the Gray-coded symbols as specified in this sub-clause when bit x in register y is set”
  - The rest of the language can stay as is
- **Add 1 control bit to the same interface as CDAUI8 c2c’s TXFIR**
  - The precoder shall be turned off by default.
  - Setting the bit will turn it on.

CONCLUSIONS

- **Bypass-able option with minimal overhead**
- **Significant improvement in performance (pre-interleaved case) with inexpensive implementation**
- **Allows FEC code word interleaving to handle other sources of correlated errors**
- **Provides lane-level mitigation against lane-level DFE generated burst errors**
  - Lane-level protection allows extension to other PAM4 AUI configurations where interleaving multiple FEC code words may not be feasible
- **No impact to an RX that doesn't need it**