Electrical Interface Ad-hoc Meeting - Opening/Agenda

IEEE P802.3bs 400Gb/s Ethernet Task Force
2nd October 2015

Opening

- The charter of the Electrical Interface Ad hoc is:
  - Address all issues in relation to the electrical interfaces to ensure progress towards a technically complete draft.
    - *Identify issues or omissions in the adopted Baselines*
    - *Find consensus now, rather than in comment resolution.*

- Next Ad-hoc Meeting
  - Provisional date : 23rd October 2015 8-10am Pacific

Patent Policy

- http://www.ieee802.org/3/patent.html

Agenda

Ad-hoc Opening/Agenda/Closing	Andre Szczepanek	szczepanek_01_100215_elect

CDAUI-8 C2C “TBD”s in Draft 0.9

- Transmitter feedback mechanism description link (120D.1)
  - No equivalent of 83D.3.3.2 in Draft 1.0
- Optional EEE support (120D.3.2)
  - If we want to to provide optional EEE support, then do we also want to support CDAUI-8 shutdown
- Receiver Jitter Tolerance row in Table 120D-4
- Table 120D-7, COM Parameters
  - Device package model:
    - Single-ended device capacitance
    - Single-ended board capacitance
  - Single-ended termination resistance

Optional Transmitter equalization feedback text from 83D.3.3.2

Transmitter equalization feedback is an optional capability for a CAUI-4 chip-to-chip receiver. If implemented, it shall operate as described in this subclause.

Transmitter equalization feedback is generated for each lane (0 through 3) and direction (transmit and receive) independently. The variables that control transmitter equalization feedback are specific for each lane and direction.

A CAUI-4 chip-to-chip receiver may generate a request to change the transmit equalization coefficients of the remote transmitter to new values by setting the *Request_flag* variable to 1. The variables *Request_eq_cm1* and *Request_eq_c1* indicate the request values of *Local_eq_cm1* and *Local_eq_c1*, respectively, in the remote transmitter (see Table 83D–2 and Table 83D–3). The requested setting may be generated from the remote CAUI-4 chip-to-chip transmitter's equalization setting, which is stored in variables *Remote_eq_cm1* and *Remote_eq_c1*, and from information internal to the receiver, in an implementation specific manner.

When a CAUI-4 chip-to-chip receiver does not request a change of the remote transmitter's transmit equalization setting, it sets the *Request_flag* variable to 0. A CAUI-4 chip-to-chip receiver that does not implement transmitter equalization feedback always sets *Requests_flag* to 0.

If a Clause 45 MDIO is implemented, the variables *Request_flag, Requested_eq_cm1, Requested_eq_c1, Remote_eq_cm1,* and *Remote_eq_c1* for each lane and direction are accessible through registers 1.180 through 1.187 (see 45.2.1.97 through 45.2.1.100).

Optional EEE operation text from 83D.3.2

If the optional Energy Efficient Ethernet (EEE) capability with the deep sleep mode option is supported (see Clause 78 and 78.3), then the inter-sublayer service interface includes four additional primitives as described in 83.3 and may also support CAUI-4 shutdown.

If the EEE capability includes CAUI-4 shutdown (see 78.5.2), then when aui_tx_mode (see 83.5.11.3) is set to ALERT, the transmit direction sublayer sends a repeating 16-bit attern, hexadecimal 0xFF00, which is transmitted across the CAUI-4. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When aui_tx_mode is QUIET, the transmit direction CAUI-4 transmitter is disabled as specified below. Similarly when the received aui_tx_mode is set to ALERT, the receive direction sublayer sends a repeating 16-bit pattern, hexadecimal 0xFF00, which is transmitted across the CAUI-4. This sequence is transmitted regardless of the value of tx_bit presented by the PMA:IS_UNITDATA_i.request primitive or the rx_bit presented by the PMA:IS_UNITDATA_i.indication primitive. When the received aui_tx_mode is QUIET, the receive direction CAUI-4 transmitter is disabled as specified below.

For EEE capability with CAUI-4 shutdown, the CAUI-4 transmitter lane's differential peak-to-peak output voltage shall be less than 30 mV within 500 ns of aui_tx_mode changing to QUIET in the relevant direction. Furthermore, the CAUI-4 transmitter lane's differential peak-to-peak output voltage shall be greater than 720 mV within 500 ns of aui_tx_mode ceasing to be QUIET in the relevant direction.

Global transmit disable is optional for EEE capability. The transmit disable function shall turn off all transmitter lanes for a physically instantiated AUI in either the ingress or the egress direction. In the egress direction, the PMA may turn off all the transmitter lanes for the egress direction CAUI-4 if PEASE is asserted and aui_tx_mode is QUIET. In the ingress direction, the PMA may turn off all the transmitter lanes for the ingress direction CAUI-4 if PIASE is asserted and the received aui_tx_mode is QUIET. In both directions, the transmit disable function shall turn on all transmitter lanes after the appropriate direction aui_tx_mode changes to any state other than QUIET within a time and voltage level specified in this subclause.

Jitter Tolerance TBD

83D.3.3 CAUI-4 receiver characteristics

A CAUI-4 chip-to-chip receiver shall meet the specifications defined in Table 83D–4 if measured at TP5a.

Table 83D–4—CAUI-4 receiver characteristics at TP5a

Parameter	Subclause reference	Value	Units
Differential input return loss (min)	93.8.2.2	Equation (93-3)	dB
Differential to common mode input return loss	93.8.2.2	Equation (93-5)	dB
Interference tolerance	83D.3.3.1	Table 83D–5	—

120D.3.3 CDAUI-8 receiver characteristics

A CDAUI-8 chip-to-chip receiver shall meet the specifications defined in Table 120D–4 if measured at TP5a.

Table 120D–4—CDAUI-8 receiver characteristics at TP5a

Parameter	Subclause reference	Value	Units
Differential input return loss (min)	93.8.1.4	Equation (93-3)	dB
Differential to common mode input return loss	93.8.1.4	Equation (93-5)	dB
Interference tolerance	120D.3.3.1	Table 120D–5	—
Jitter tolerance	120D.3.3.2	TBD	—

Table 120D-7: COM Parameters

Table 120D–7—Channel Operating Margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	26.5625	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length, Test 1 Transmission line length, Test 2 Single-ended board capacitance	 C_d z_p z_p C_b	 TBD 12 30 TBD	 nF mm mm nF
Single-ended reference resistance	R_o	50	ohms
Single-ended termination resistance	R_d	TBD	ohms

Annex 120E (CDAUI-8 C2M) “TBD”s in Draft 0.9

Annex 120E (CDAUI-8 C2M)

- Transition time
- Host stressed input pattern generator jitter characteristics (Table 120E-5)
- Single-ended voltage tolerance range (min)
- Module stressed input Pattern generator jitter characteristics (Table 120E-8)

Transition time (one example)

Table 120E–1—CDAUI-8 host output characteristics (at TP1a)

Parameter	Reference	Value	Units
Signaling rate per lane (range)	120E.3.1.1	26.5625 ± 100 ppm	GBd
DC common-mode output voltage (max)	120E.3.1.2	2.8	V
DC common-mode output voltage (min)	120E.3.1.2	–0.3	V
Single-ended output voltage (max)	120E.3.1.2	3.3	V
Single-ended output voltage (min)	120E.3.1.2	–0.4	V
AC common-mode output voltage (max, RMS)	120E.3.1.2	17.5	mV
Differential peak-to-peak output voltage (max) Transmitter disabled Transmitter enabled	120E.3.1.2	 35 900	mV
Eye width[a] (min)	120E.4.2	0.25	UI
Eye height A[b], differential (min)	120E.4.2	50	mV
Differential output return loss (min)	83E.3.1.3	Equation (83E-2)	dB
Common to differential mode conversion return loss (min)	83E.3.1.3	Equation (83E-3)	dB
Differential termination mismatch (max)	120E.3.1.4	10	%
Transition time (min, 20% to 80%)	120E.3.1.5	TBD	ps

Stressed input Pattern generator characteristics

Table 120E–5—Pattern generator jitter characteristics

Parameter	Value
Total Jitter (pk-pk)[a]	TBD UI
Random Jitter (pk-pk)[b]	TBD UI
Max even-odd jitter (pk-pk)[c]	TBD UI

[a]Total Jitter at BER of 10^{-6}
[b]Random Jitter at BER of 10^{-6}
[c]As defined in 92.8.3.8.1

Table 120E–8—Pattern generator jitter characteristics

Parameter	Value
Total Jitter (pk-pk)[a]	TBD UI
Random Jitter (pk-pk)[b]	TBD UI
Max even-odd jitter (pk-pk)[c]	TBD UI

[a]Total Jitter at BER of 10^{-6}.
[b]Random Jitter at BER of 10^{-6}.
[c]As defined in 92.8.3.8.1.

Single-ended voltage tolerance range (min)

Table 120E–6—CDAUI-8 module input characteristics *(continued)*

Parameter	Reference	Test point	Value	Units
Module stressed input test[a]	120E.3.4.1	TP1a	See 120E.3.4.1	
Single-ended voltage tolerance range (min)	120E.3.1.2	TP1a	TBD	V
DC common mode voltage (min)[b]	120E.3.1.2	TP1	–350	mV
DC common mode voltage (max)[b]	120E.3.1.2	TP1	2850	mV

[a]Meets BER specified in 120E.1.1.
[b]DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Discussion

Backup

Participants, Patents, and Duty to Inform

All participants in this meeting have certain obligations under the IEEE-SA Patent Policy.

- **Participants [Note: Quoted text excerpted from IEEE-SA Standards Board Bylaws subclause 6.2]:**
  - **"Shall inform the IEEE (or cause the IEEE to be informed)" of the identity of each "holder of any potential Essential Patent Claims of which they are personally aware" if the claims are owned or controlled by the participant or the entity the participant is from, employed by, or otherwise represents**
  - **"Should inform the IEEE (or cause the IEEE to be informed)" of the identity of "any other holders of potential Essential Patent Claims" (that is, third parties that are not affiliated with the participant, with the participant's employer, or with anyone else that the participant is from or otherwise represents)**
- **The above does not apply if the patent claim is already the subject of an Accepted Letter of Assurance that applies to the proposed standard(s) under consideration by this group**
- **Early identification of holders of potential Essential Patent Claims is strongly encouraged**
- **No duty to perform a patent search**

Patent Related Links

All participants should be familiar with their obligations under the IEEE-SA Policies & Procedures for standards development.

Patent Policy is stated in these sources:

IEEE-SA Standards Boards Bylaws

http://standards.ieee.org/develop/policies/bylaws/sect6-7.html#6

IEEE-SA Standards Board Operations Manual

http://standards.ieee.org/develop/policies/opman/sect6.html#6.3

Material about the patent policy is available at

http://standards.ieee.org/about/sasb/patcom/materials.html

If you have questions, contact the IEEE-SA Standards Board Patent Committee Administrator at patcom@ieee.org or visit http://standards.ieee.org/about/sasb/patcom/index.html

This slide set is available at https://development.standards.ieee.org/myproject/Public/mytools/mob/slideset.ppt

Call for Potentially Essential Patents

- If anyone in this meeting is personally aware of the holder of any patent claims that are potentially essential to implementation of the proposed standard(s) under consideration by this group and that are not already the subject of an Accepted Letter of Assurance:
  - Either speak up now or
  - Provide the chair of this group with the identity of the holder(s) of any and all such claims as soon as possible or
  - Cause an LOA to be submitted